LATCH UP TEST REPORT

Company ：成都启英泰伦科技有限公司

Address ：成都市高新区天府五街 **200** 号菁蓉汇 **4A** 栋 **12** 楼

Model Name ：**CI1122**

Date Received ：October 15, 2020

Date Tested ：October 15, 2020

TESTING LABORATORY IS APPROVEDED BY:

IECQ Certificate of Approval No.: IECQ-L DEKRA 17.0004-01 For Independent Test Laboratory According to ISO/IEC 17025

WE HEREBY CERTIFY THAT:

The test(s) shown in the attachment were conducted according to the indicating procedures. We assume full responsibility for the accuracy and completeness of these tests and vouch for the qualifications of all personnel performing them.

	Name	Signature	Date
Testing Engineer	Peng_Zhao	Peng_Zhao	2020/10/15
Approving Manager	Kimi Lai	Kimi_Lai	2020/10/15

Note：

1. This report will be invalid if reproduced in whole or in part.
2. This report refers only to the specimen(s) submitted to test, and is invalid if used separately.
3. This report is ONLY valid with the examination seal and signature of this institute.
4. The tested specimen(s) will only be preserved for thirty days from the date issued, if not collected by the applicant.
5. The failure criteria of all ESD tests should be based on the result of parametric and functional testing conducted by the customer, which follows the statement of international standards. Thus, the judgment of the curve traces provided in this report is for reference ONLY.

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1. GENERAL INFORMATION

1.1 DESCRIPTION OF UNIT

MANUFACTURER	：成都启英泰伦科技有限公司
DEVICE NAME	：CI1122
PACKAGED / PIN COUNT	：QFN48 6x6mm
REFERENCE DOCUMENT	：JEDEC STANDARD NO.78E NOVEMBER 2016
TRIGGER CURRENT	：50mA~200mA,STP:50mA(±)
V SUPPLY OVER VOLTAGE TEST	：3.5V~5.5V,STEP:1.0V(+) ：1.32V~1.98V,STEP:0.2V(+)
PULSE DURATION	：10 ms
TEST TEMPERATURE	：ROOM TEMPERATURE
SAMPLE QUANTITY	：3 pcs
FAILURE CRITERIA	：If absolute Inom is < 25 mA, then absolute Inom + 10mA is used; Or If absolute Inom is > 25 mA, then > 1.4X absolute Inom is used;

2. LATCH UP TEST

2.1 TEST EQUIPMENT

Test Equipment	Equipment S/N	Calibration Date:	Recommended Due Date:
KEYTEK ZAPMASTER 7/4	0008189	July 7, 2020	July 6, 2021

2.2 LABORATORY AMBIENCE CONDITION

Temperature：25±5°C

Relative humidity：55%±10% (RH)

2.3 REFERENCE DOCUMENT

The test is based on JEDEC STANDARD NO.78E NOVEMBER 2016

2.4 TEST CONDITION

I Trigger：

Over Voltage Test：

2.5 SUMMARY OF TEST

Trigger Mode	Test Pin	Sample Quantity	Tested Result	V or I Limits	I Trigger : Class ⅠA
I Trigger (+)	I/P3.63V	3	PASS +200mA	+5.445V	**Temperature Classification:** CLASSⅠ: For Latch-up test at room temperature CLASSⅠA≧100mA CLASSⅠB＜100mA CLASSⅡ: For Latch-up test at maximum-rate ambient temperature CLASSⅡA≧100mA CLASSⅡB＜100mA
	O/P3.63V		PASS +200mA	+5.445V	
	BI/O3.63V		PASS +200mA	+5.445V	
I Trigger (-)	I/P3.63V		PASS -200mA	-1.815V	
	O/P3.63V		PASS -200mA	-1.815V	
	BI/O3.63V		PASS -200mA	-1.815V	
Over Volt Test V_{supply}	VDD3.63V		PASS +5.5V	+600mA	
	VDD1.32V		PASS +1.98V	+600mA	

I/P3.63V	1,24-25,37-38
O/P3.63V	39,43,45-46,48
BI/O3.63V	4-7,10-20,22-23,26-27,30-36,47
VDD3.63V	8,21,28,41,44
VDD1.32V	2,9,29
VSS	3,40,42,49

2.6 CONTENTS OF TEST

I Trigger (Positive)							
Tested Pin	Sample No. & Failed current (mA)			Tested Pin	Sample No. & Failed current (mA)		
	#4	#5	#6		#4	#5	#6
1	PASS	PASS	PASS	15	PASS	PASS	PASS
24	PASS	PASS	PASS	16	PASS	PASS	PASS
25	PASS	PASS	PASS	17	PASS	PASS	PASS
37	PASS	PASS	PASS	18	PASS	PASS	PASS
38	PASS	PASS	PASS	19	PASS	PASS	PASS
39	PASS	PASS	PASS	20	PASS	PASS	PASS
43	PASS	PASS	PASS	22	PASS	PASS	PASS
45	PASS	PASS	PASS	23	PASS	PASS	PASS
46	PASS	PASS	PASS	26	PASS	PASS	PASS
48	PASS	PASS	PASS	27	PASS	PASS	PASS
4	PASS	PASS	PASS	30	PASS	PASS	PASS
5	PASS	PASS	PASS	31	PASS	PASS	PASS
6	PASS	PASS	PASS	32	PASS	PASS	PASS
7	PASS	PASS	PASS	33	PASS	PASS	PASS
10	PASS	PASS	PASS	34	PASS	PASS	PASS
11	PASS	PASS	PASS	35	PASS	PASS	PASS
12	PASS	PASS	PASS	36	PASS	PASS	PASS
13	PASS	PASS	PASS	47	PASS	PASS	PASS
14	PASS	PASS	PASS	-----	-----	-----	-----

I Trigger (Negative)							
Tested Pin	Sample No. & Failed current (mA)			Tested Pin	Sample No. & Failed current (mA)		
	#4	#5	#6		#4	#5	#6
1	PASS	PASS	PASS	15	PASS	PASS	PASS
24	PASS	PASS	PASS	16	PASS	PASS	PASS
25	PASS	PASS	PASS	17	PASS	PASS	PASS
37	PASS	PASS	PASS	18	PASS	PASS	PASS
38	PASS	PASS	PASS	19	PASS	PASS	PASS
39	PASS	PASS	PASS	20	PASS	PASS	PASS
43	PASS	PASS	PASS	22	PASS	PASS	PASS
45	PASS	PASS	PASS	23	PASS	PASS	PASS
46	PASS	PASS	PASS	26	PASS	PASS	PASS
48	PASS	PASS	PASS	27	PASS	PASS	PASS
4	PASS	PASS	PASS	30	PASS	PASS	PASS
5	PASS	PASS	PASS	31	PASS	PASS	PASS
6	PASS	PASS	PASS	32	PASS	PASS	PASS
7	PASS	PASS	PASS	33	PASS	PASS	PASS
10	PASS	PASS	PASS	34	PASS	PASS	PASS
11	PASS	PASS	PASS	35	PASS	PASS	PASS
12	PASS	PASS	PASS	36	PASS	PASS	PASS
13	PASS	PASS	PASS	47	PASS	PASS	PASS
14	PASS	PASS	PASS	-----	-----	-----	-----

Over Voltage Test for V_{supply}			
Tested Pin	Sample No. & Failed Volt (V)		
	#4	#5	#6
8	PASS	PASS	PASS
21	PASS	PASS	PASS
28	PASS	PASS	PASS
41	PASS	PASS	PASS
44	PASS	PASS	PASS
2	PASS	PASS	PASS
9	PASS	PASS	PASS
29	PASS	PASS	PASS