华测蔚思博检测
CTI-VESP Technology Corp.

Report No.：VWO5-23080056-LU
Report Ver.：01
Report Date：2023/08/16

CTI-VESP Technology Corporation

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LATCH UP Test Report

Testing laboratory is accredited by

IEC quality assessment system (IECQ)：ISO/IECQ 17025 (Certificate No.：IECQ-L ULTW 21.0001)

	Signature	Date
Testing Engineer		*2023/08/16*
Technical Manager		*2023/08/16*
Approval Manager		*2023/08/16*

NOTE：

- This report is generated subject to certain conditions (including but not limited to: designated samples, designated environment parameters and designated input signals). VESP Technology Co., Ltd. does not guarantee that the test results under different conditions or generated by other people will coincide with this report.
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- VESP Technology Co., Ltd. is not responsible for whether the samples tested in this report will function well as their original design and/or meet any expectation.

1. Application Information：

1.1 Test Items：LATCH-UP (LU)

1.2 Test Serial No.：VWO5-23080056

2. Customer Basic Information：

2.1 Company：Chipintelli Technology Co., Ltd.

2.2 Applicant：DaoMin Li

2.3 Address：The 12th floor,Building 4A, Jingronghui, No.200 Tianfu 5th Street, High-tech Zone, Chengdu, China.

2.4 Package/Pin Count：TSSOP/24

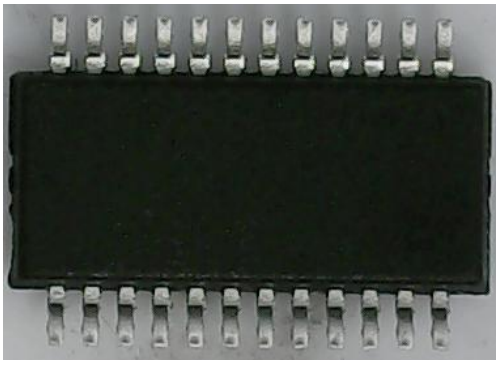
2.5 Application Date：2023/08/02

2.6 Tested Date：2023/08/02

2.7 Device Information：

Device Name	Lot No.	Sample Q’ ty (ea)
CI1302	BD0230	3

2.8 Device Photos：

Top View	Bottom View
	

3. Environmental Conditions of Laboratory：

3.1 Temperature：23.5°C

3.2 Humidity：50.2% R.H.

4. Test Equipment：

4.1 Test Item：LATCH-UP

4.2 Test Equipment：

Item	Test Equipment	Serial No.	Calibration Expiration
LATCH-UP	HANWA HED-N5000	653177	2023/09/04

5. Test Procedure：

5.1 Reference Specification：JESD78E-2016

5.2 Test Procedure and Conditions：

5.2.1 Test Condition:

+ Current Trigger

- Current Trigger

Vsupply Over-voltage test

5.2.2 Failure Criteria: <25mA: 10mA+Inom、 >25mA: 1.4 x Inom

5.2.3 Trigger Current: ±50mA ~±200mA, Step: 50mA

5.2.4 Bias Description

VIN 4V=4.5V(max), GND=0V

I/P Bias at High; I/P Bias at Low (trigger one time on each bias state)

5.3 Pin Assignment：

VIN 4V: 2

VCC 3.3V: 1,3
VDD 1.1V: 4
GND: 5,8
AGND: 24
IP 3.3V: 18,19,20,21
OP 1.6V: 23
OP 2.8V: 22
OP 3.3V: 17
IO 3.3V: 6,7,9,10,11,12,13,14,15,16

6. Test Result：

Room temp.

TRIGGER MODEL	TEST PIN	SAMPLE SIZE	PASS Vol./Cur.	V or I Limits	CLASS: I
+IT	IP 3.3V	3	+200mA	5.4V	NOTE: JESD78E-2016
	OP 1.6V		+200mA	2.4V	I:Room temp.
	OP 2.8V		+200mA	4.2V	II:High temp.
	OP 3.3V		+200mA	5.4V	
	IO 3.3V		+200mA	5.4V	
-IT	IP 3.3V		-200mA	-1.8V	
	OP 1.6V		-200mA	-0.8V	
	OP 2.8V		-200mA	-1.4V	
	OP 3.3V		-200mA	-1.8V	
	IO 3.3V		-200mA	-1.8V	
V supply OVER VOLTAGE TEST	VIN 4V		6.75V	600mA	

7. Special Remarks：NA

8. Attachment：

LATCH-UP：(±)Current Trigger Modes

(Unit:mA)

Test Mode	(+)IT Mode		
Pass Voltage / Pin Name	#L1	#L2	#L3
1	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)
3	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)
4	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)
6	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)
7	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)
9	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)
10	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)
11	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)
12	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)
13	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)
14	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)
15	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)

(Unit:mA)

Test Mode	(-)IT Mode		
Pass Voltage / Pin Name	#L1	#L2	#L3
1	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)
3	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)
4	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)
6	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)
7	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)
9	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)
10	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)
11	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)
12	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)
13	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)
14	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)
15	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)

16	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)
17	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)
18	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)
19	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)
20	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)
21	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)
22	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)
23	PASS (+200mA)	PASS (+200mA)	PASS (+200mA)

16	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)
17	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)
18	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)
19	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)
20	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)
21	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)
22	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)
23	PASS (-200mA)	PASS (-200mA)	PASS (-200mA)

The tested Sample (units) was complied with test Current ±200mA, I-V curve shift ≤ 30%.

LATCH-UP：Vsupply OVERVOLTAGE TEST Modes

(Unit：Volt)

Test Mode	Vsupply OVERVOLTAGE TEST Mode		
Pass Voltage / Pin	#L1	#L2	#L3
2	PASS(6.75V)	PASS(6.75V)	PASS(6.75V)

The tested Sample (units) was complied with test Voltage 6.75V, I-Vcurve shift ≤ 30%.

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