

ESD (HUMAN BODY MODE) TEST REPORT

Company : 成都启英泰伦科技有限公司Address : 成都市高新区天府五街 200 号菁蓉汇 4A 栋 12 楼Model Name : CI1122Date Received : October 15, 2020Date Tested : October 15, 2020

TESTING LABORATORY IS APPROVED BY:

IECQ Certificate of Approval No.: IECQ-L DEKRA 17.0004-01 For Independent Test Laboratory
According to ISO/IEC 17025

WE HEREBY CERTIFY THAT:

The test(s) shown in the attachment were conducted according to the indicating procedures.
We assume full responsibility for the accuracy and completeness of these tests and vouch
for the qualifications of all personnel performing them.

	Name	Signature	Date
Testing Engineer	Peng_Zhao	<i>Peng_Zhao</i>	2020/10/15
Approving Manager	Kimi Lai	<i>Kimi_Lai</i>	2020/10/15

Note :

1. This report will be invalid if reproduced in whole or in part.
2. This report refers only to the specimen(s) submitted to test, and is invalid if used separately.
3. This report is ONLY valid with the examination seal and signature of this institute.
4. The tested specimen(s) will only be preserved for thirty days from the date issued, if not collected by the applicant.
5. The failure criteria of all ESD tests should be based on the result of parametric and functional testing conducted by the customer, which follows the statement of international standards. Thus, the judgment of the curve traces provided in this report is for reference ONLY.



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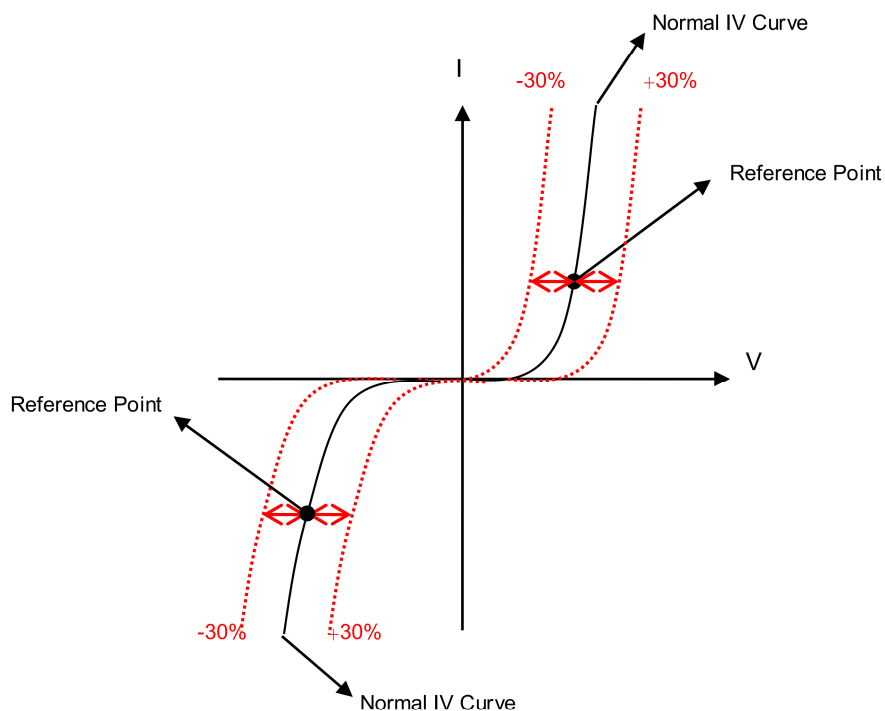
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1. GENERAL INFORMATION

1.1 DESCRIPTION OF UNIT

MANUFACTURER : 成都启英泰伦科技有限公司
DEVICE NAME : CI1122
PACKAGED / PIN COUNT : QFN48 6x6mm
REFERENCE DOCUMENT : ANSI/ESDA/JEDEC JS-001-2017 Zap 1 pulse(s), Interval: 0.3 Sec.
TEST VOLTAGE : 2000V(±), 3000V(±), 4000V(±), 5000V(±), 6000V(±), 7000V(±), 8000V(±);
SAMPLE QUANTITY : 3 pcs
FAILURE CRITERIA (Reference Only) : ±30% voltage shift at reference point before/after zapping

※ Failure Judgment: Voltage shift over ±30% at reference point.



2. ESD (HUMAN BODY MODE) TEST

2.1 TEST EQUIPMENT

Test Equipment	Equipment S/N	Calibration Date:	Recommended Due Date:
KEYTEK ZAPMASTER 7/4	0008189	July 7, 2020	July 6, 2021

2.2 LABORATORY AMBIENCE CONDITION

Temperature : 25±5°C

Relative humidity : 55%±10% (RH)

2.3 REFERENCE DOCUMENT

The test is based on ANSI/ESDA/JEDEC JS-001-2017

2.4 TEST CONDITION

All other pins to VSS (+/-)

All other pins to PLL_AVSS12 (+/-)

All other pins to AGND (+/-)

All other pins to VCC33 (+/-)

All other pins to VCC12 (+/-)

All other pins to PLL_AVDD12 (+/-)

All other pins to AVDD (+/-)

IO TO IO (+/-)

Step:2000V, 3000V, 4000V, 5000V, 6000V, 7000V, 8000V

2.5 SUMMARY OF TEST

Test Model : HBM	ESD Sensitivity Passed : $\pm 4000V$		ANSI/ESDA/JEDEC JS-001-2017 Classification Class : <u>3A</u>
Test condition	Sample Quantity	Passed Volts	Class 0Z : < 50V Class 0A : $\geq 50V$, < 125V Class 0B : $\geq 125V$, < 250V Class 1A : $\geq 250V$, < 500V Class 1B : $\geq 500V$, < 1000V Class 1C : $\geq 1000V$, < 2000V Class 2 : $\geq 2000V$, < 4000V Class 3A : $\geq 4000V$, < 8000V Class 3B : $\geq 8000V$
All other pins to VSS (+/-) All other pins to PLL_AVSS12 (+/-) All other pins to AGND (+/-) All other pins to VCC33 (+/-) All other pins to VCC12 (+/-) All other pins to PLL_AVDD12 (+/-) All other pins to AVDD (+/-) IO TO IO (+/-) Step:2000V, 3000V, 4000V, 5000V, 6000V, 7000V, 8000V	3	$\pm 4000V$	

Group	Pins
AGND	40,42
AVDD	41,44
AVDD1	41
AVDD2	44
IO	1,4-7,10-20,22-27,30-39,43,45-48
PLL_AVDD12	2
PLL_AVSS12	3
VCC12	9,29
VCC33	8,21,28
VSS	49

2.6 CONTENTS OF TEST

No	1		
	All other pins to VSS (+/-) All other pins to PLL_AVSS12 (+/-) All other pins to AGND (+/-) All other pins to VCC33 (+/-) All other pins to VCC12 (+/-) All other pins to PLL_AVDD12 (+/-) All other pins to AVDD (+/-) IO TO IO (+/-) Step:2000V, 3000V, 4000V, 5000V, 6000V, 7000V, 8000V		
Tested Pins	Sample No. & Failed Volt		
	#01	#02	#03
1	FAIL(8000V)	FAIL(8000V)	PASS(8000V)
2	PASS(8000V)	PASS(8000V)	PASS(8000V)
3	FAIL(8000V)	FAIL(8000V)	PASS(8000V)
4	PASS(8000V)	PASS(8000V)	PASS(8000V)
5	PASS(8000V)	PASS(8000V)	PASS(8000V)
6	PASS(8000V)	PASS(8000V)	PASS(8000V)
7	PASS(8000V)	PASS(8000V)	PASS(8000V)
8	FAIL(8000V)	FAIL(8000V)	PASS(8000V)
9	FAIL(8000V)	PASS(8000V)	PASS(8000V)
10	FAIL(8000V)	PASS(8000V)	PASS(8000V)
11	FAIL(8000V)	PASS(8000V)	PASS(8000V)
12	FAIL(8000V)	PASS(8000V)	PASS(8000V)
13	FAIL(8000V)	PASS(8000V)	PASS(8000V)
14	FAIL(8000V)	PASS(8000V)	PASS(8000V)
15	FAIL(8000V)	PASS(8000V)	PASS(8000V)
16	FAIL(8000V)	PASS(8000V)	PASS(8000V)
17	FAIL(8000V)	PASS(8000V)	PASS(8000V)
18	FAIL(8000V)	PASS(8000V)	PASS(8000V)
19	FAIL(8000V)	FAIL(8000V)	PASS(8000V)
20	FAIL(8000V)	FAIL(8000V)	PASS(8000V)
21	FAIL(8000V)	FAIL(8000V)	PASS(8000V)
22	FAIL(8000V)	PASS(8000V)	PASS(8000V)
23	FAIL(8000V)	PASS(8000V)	PASS(8000V)
24	FAIL(8000V)	PASS(8000V)	PASS(8000V)
25	FAIL(8000V)	PASS(8000V)	PASS(8000V)
26	FAIL(8000V)	PASS(8000V)	PASS(8000V)
27	FAIL(8000V)	PASS(8000V)	PASS(8000V)
28	FAIL(8000V)	FAIL(8000V)	PASS(8000V)
29	FAIL(8000V)	PASS(8000V)	PASS(8000V)
30	FAIL(8000V)	PASS(8000V)	PASS(8000V)
31	FAIL(8000V)	PASS(8000V)	PASS(8000V)
32	FAIL(8000V)	PASS(8000V)	PASS(8000V)
33	FAIL(8000V)	PASS(8000V)	PASS(8000V)
34	FAIL(8000V)	PASS(8000V)	PASS(8000V)
35	FAIL(8000V)	PASS(8000V)	PASS(8000V)
36	FAIL(8000V)	PASS(8000V)	PASS(8000V)
37	PASS(8000V)	PASS(8000V)	PASS(8000V)
38	PASS(8000V)	PASS(8000V)	PASS(8000V)

39	PASS(8000V)	PASS(8000V)	PASS(8000V)
40	FAIL(8000V)	FAIL(8000V)	PASS(8000V)
41	PASS(8000V)	PASS(8000V)	PASS(8000V)
42	FAIL(8000V)	FAIL(8000V)	PASS(8000V)
43	FAIL(5000V)	FAIL(5000V)	FAIL(5000V)
44	PASS(8000V)	PASS(8000V)	PASS(8000V)
45	PASS(8000V)	PASS(8000V)	PASS(8000V)
46	PASS(8000V)	PASS(8000V)	PASS(8000V)
47	PASS(8000V)	PASS(8000V)	PASS(8000V)
48	PASS(8000V)	PASS(8000V)	PASS(8000V)
49	FAIL(8000V)	FAIL(8000V)	PASS(8000V)