CI13082V Data Sheet

High cost performance neural network intelligent voice chip

- **Brain Neural Network Processor (BNPU)**

-BNPU V3.5, supports DNN\TDNN\RNN\CNN and other neural networks and parallel vector operations, can achieve high performance speech recognition and call noise reduction and other functions

CPU and memory

-CPU frequency up to 210 MHz

-Built-in 2MBytes Flash memory

-Built-in 288KBytes SRAM

-Built-in 256-bit eFuse for application encryption

- **Audio Codec**

-High performance low power consumption audio ADC, SNR ≥ 95dB

-Low power consumption audio DAC, SNR ≥ 95dB

- **PWM**

-Supports 3 PWM interfaces

- **GPIO**

-3 high-speed GPIO with a flip frequency of up to 20MHz

-2 GPIO channels support 5V level communication

- **Reset and power management**

-Power supply voltage 3.3V

-Built-in PMU power management unit

-Built-in power-on reset (POR)

-Built-in voltage detection (PVD)

- **clock**

-Built-in RC oscillator

- **communication interface**

-1 IIC interface

-1 UART interface, supports 5V level communication, up to 3Mbps communication rate

- **Timer and watchdog**

-Built-in 2 sets of 32-bit timers and 1 watchdog

catalogue

1 Summary

1.1 Functional description

CI13082V is a new generation of high-performance neural network intelligent voice chip developed by Chipintelli, which integrates Chipintelli's Brain Neural Network Processor (BNPU) V3.5 and CPU core, featuring a clock speed of up to 210MHz. It incorporates 288KB of SRAM, a Power Management Unit (PMU), and a RC oscillator. The design also includes a single-channel high-performance, low-power Audio Codec along with multiple peripheral control interfaces such as UART, IIC, PWM, and GPIO. The CI13082V chip requires only minimal resistors and capacitors to implement hardware solutions for various intelligent voice products, delivering exceptional cost-effectiveness.

CI13082V adopts industrial design standards, has good environmental reliability, its working temperature range-40℃ ～+85℃, in line with MSL3 moisture sensitivity level, in line with IEC 61000-4-24KV contact discharge test standard, in line with RoHS and REACH environmental standards.

The CI13082V leverages Chipintelli's next-generation BNPU technology, which supports neural networks (DNN/TDNN/RNN/CNN) and parallel vector operations. This enables high-performance speech recognition, noise reduction, and exceptional environmental noise suppression capabilities. The CI13082V solution supports multiple global languages including Chinese, English, and Japanese, making it widely applicable across industries such as home appliances, lighting, toys, wearables, industrial equipment, and automotive sectors. It facilitates voice interaction control and supports various intelligent voice application scenarios.

1.2 Chip specifications

The function block diagram of CI13082V is shown in Figure 1-1:

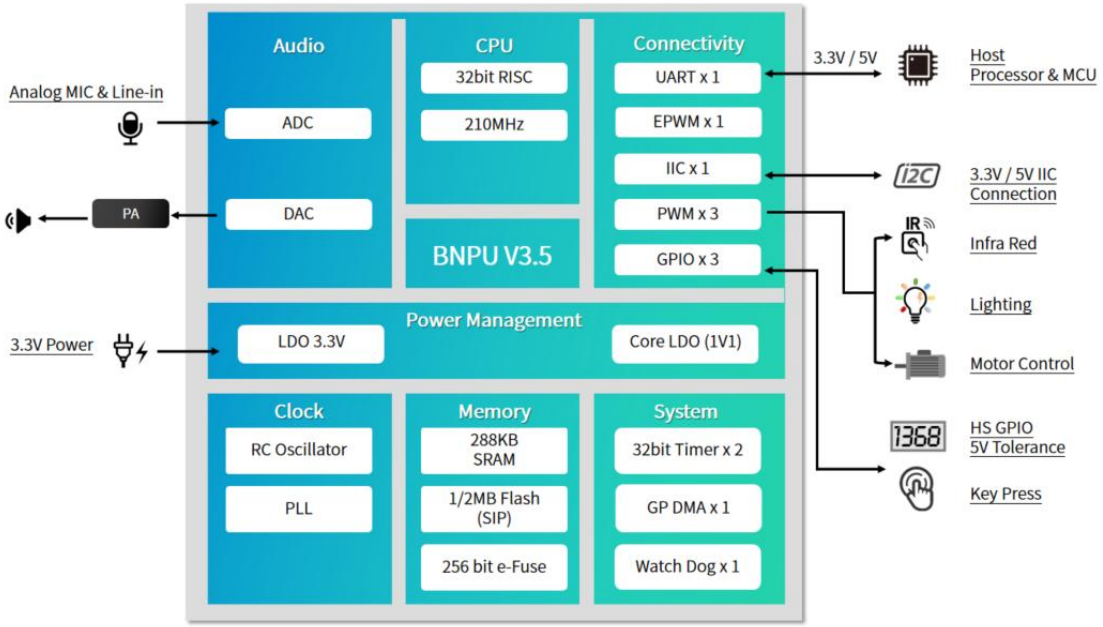


Figure 1-1 CI13082V function block diagram

- **Brain network processor BNPU V3.5**

-It adopts the new generation hardware BNPU technology of Chipintelli, which supports DNN\TDNN\RNN\CNN and other neural networks as well as parallel vector operation, and can realize high performance speech recognition, speech noise reduction and other functions

- **CPU**

-32-bit high performance CPU, up to 210MHz operating frequency

- **Memory**

-Built-in 288KB SRAM

-Built-in 256bit eFuse

-Built-in 2MB Flash

- **Audio interface**

-Built-in high performance low power Audio Codec module, support single channel ADC sampling and single channel DAC playback

-Support for Automatic Level Control (ALC)

-Support for 8kHz/16kHz/24kHz/32kHz/44.1kHz/48kHz sampling rate

- **Power management unit PMU**

-Supply voltage 3.3V

-Built-in 2 high performance LDO circuits, no need to configure external power chip, application scheme only needs a small number of peripheral components

- **Clock**

-Built-in RC oscillator

- **External devices and timers**

-1 UART interface, support up to 3M baud rate communication

-1 IIC interface, which can be connected to IIC devices for expansion

-3 PWM interfaces, which can be directly driven for lamp control and motor applications

-Built-in 2 sets of 32bit timers

-Built-in 1 independent watchdog (IWDG)

- **GPIO**

-Supports 3 GPIO ports and can be used as master IC

-Each GPIO port can be configured with interrupt function and pull-up/down state

-2 GPIO channels can directly support 5V level communication through an external 5V pull-up resistor

- **Software development support**

-Provide complete software development kits, application solution examples, direct online firmware development using the voice development platform and other support. For details, please visit: https://aiplatform.chipintelli.com

- **Firmware programming and protection**

-Support UART upgrade and firmware protection

- **ESD**

-Internal ESD enhanced design, which can pass the 4KV contact discharge test

- **ROHS and REACH**

-Use of environmentally friendly materials, support RoHS and REACH standards

- **Encapsulation and operating temperature range**

-Packaging form: SOP8, size of 4.9mm long, 6.0mm wide and 1.75mm high

-Working environment temperature: -40℃ ～+85℃

2 Pin diagram and function description

2.1 Pin diagram

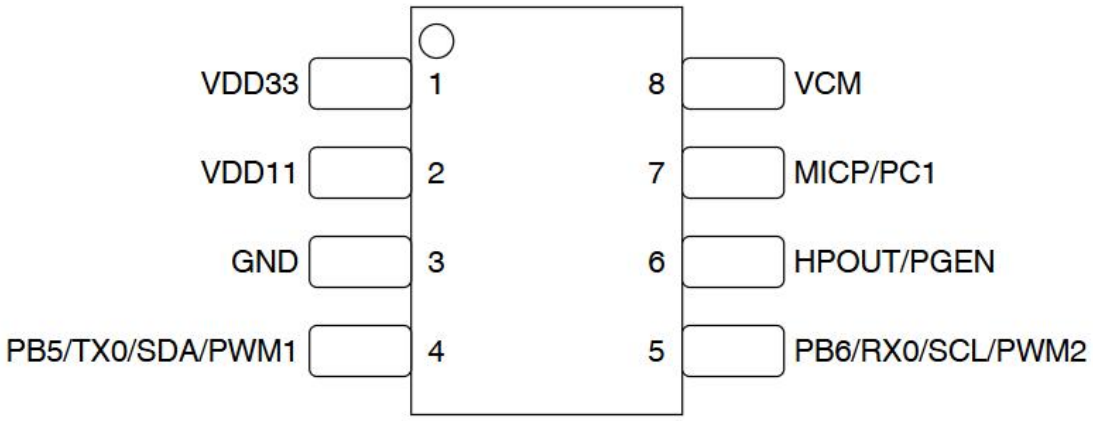


Figure 2-1 CI13082V pin sequence and definition Figure

2.2 Pin Description

Pin description Table 2-1

Pin Number	Pin Name	Type	5V Tolerant	Power-on Default State	Pin Function
1	VDD33	P	-	-	● LDO-3.3V output ● Analog 3.3V powered input * Note1*
2	VDD11	P	-	-	● LDO-1.1V output ● The kernel has a 1.1V power supply input * Note1*
3	GND	P	-	-	Ground
4	PB5	IO	√	IN，T+U	● GPIO PB5 (default state on power on) ● UART0_TX ● IIC_SDA ● PWM1 ● PWMP
5	PB6	IO	√	IN，T+U	● GPIO PB6 (default on power up) ● UART0_RX ● IIC_SCL ● PWM2 ● PWMN
6	HPOUT	O	-	-	● DAC output ● PC0 ● - ● - ● PWM0 ● PGEN * Note2*
7	MICP	I	-	-	● Microphone P input ● GPIO PC1 ● TX2 ● PWM3
8	VCM	P	-	-	VCM voltage, external 4.7uf capacitor

Note1 The pin needs to be connected to a 4.7uF capacitor

Note2 The pin is high when powered on and the system will enter programming mode

Symbol definition:

I import I import

O output O output

IO two-way IO two-way

P Power or ground P Power or ground

T+D three-state down T+D three-state down

T+U Tri-State Pull-Up T+U Tri-State Pull-Up

OUT The default output of the power supply

IN Upper default input

All IOs can be configured with drive capability and pull-up/down status.

2.3 IO Multiplexing Functionality

Table 2-2 IO multiplexing functions

Pin Name	Function1	Function2	Function3	Function4	Function5	Function6	Specific Function
PB5	PB5	UART0_TX	IIC_SDA	PWM1	PWMP		
PB6	PB6	UART0_RX	IIC_SCL	PWM2	PWMN		
PC1	-	PC1	TX2	PWM3			
PC0 * Note3*	PC0	-	-	PWM0			PGEN

Note 3: The HPOUT and PC0 (PGEN) pins are multiplexed with default internal pull-down functionality, which can be configured through software after power-on. When the system detects a high-level signal on this pin and receives a firmware upgrade command from the UART0 interface during power-up, it automatically enters upgrade mode, allowing programming of the chip's internal Flash memory via an upgrade tool. If no firmware upgrade signal is detected on the UART0 interface or the PC0 pin voltage remains low, normal operation mode will be activated.

3 Electrical character

Table 3-1 Electrical characteristics table

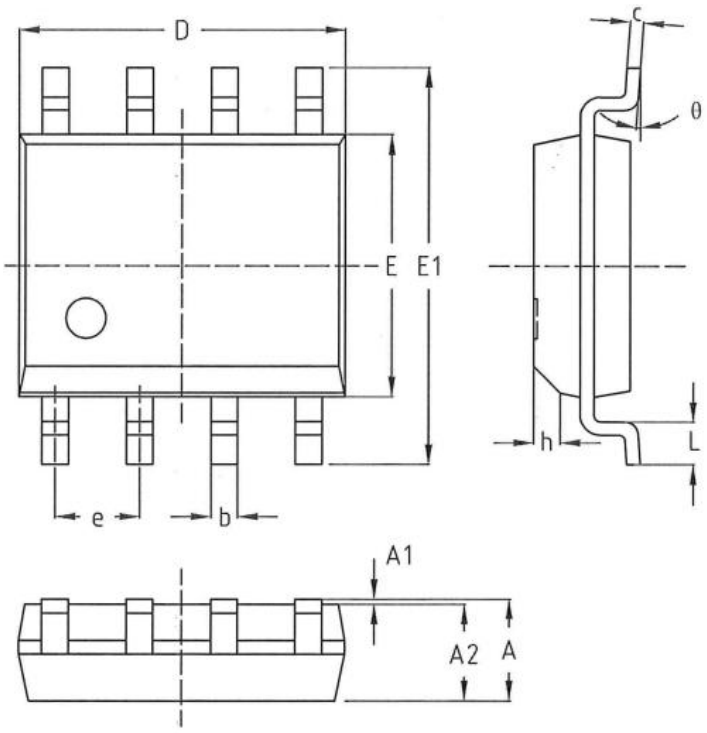
Symbol	Description	Min	Type	Max	Unit
VDD33	3.3V power supply	3.0	3.3	3.6	V
VDD11	1.1V power supply	0.99	1.1	1.21	V
VIH	Enter a high level （3.0V ≤VDD33 ≤ 3.6V）	0.7× VDD33	-	VDD33+0.3	V
VIL	Input low level （3.0V ≤ VDD33 ≤ 3.6V）	-0.3	-	0.3× VDD33	V
VOL	Output low level @IOL = 12mA	-	-	0.4	V
VOH	Output high level @IOH = 20mA	2.4	-	-	V
I5V-IO	Drive current at 3.3V when the 5V voltage IO port is output	20	-	33	mA
I3V3-IO	3.3V voltage withstand IO output 3.3V drive current	14	-	24	mA
ΣIVDD	The sum of all the total currents of the chip	-	-	90	mA
Pde	The chip is powered by 3.3V and VDD11 is supplied with 1.1V externally. The total power consumption of the 3.3V power supply (TA = 25 ° C) is normally recognized	40	-	90	mW
Pdi	The chip is powered by 3.3V and the system is powered by internal LDO. The total power consumption of the 3.3V input (TA = 25 ° C) is normally recognized	99	-	175	mW
Precision of RC oscillator *Note5*	TA：-40℃～+85℃	-1.5	-	+1.5	%
Top	Chip operating temperature	-40	-	+85	℃
Tst	Chip storage ambient temperature	-55	-	+150	℃

Note4: The ripple is required to be less than 100mVp-p.

Note 5: Due to the inherent characteristics of semiconductor technology, the built-in RC oscillator in the chip may exhibit temperature-dependent frequency drift (±1.5%) in extreme temperature environments. The CI13082V chip incorporates a baud rate adaptive circuit that ensures stable

communication between the chip and host computer across varying temperatures. For applications requiring ultra-precise clock synchronization, please utilize our externally oscillator-equipped chips with corresponding customized solutions.

4 Packaging information

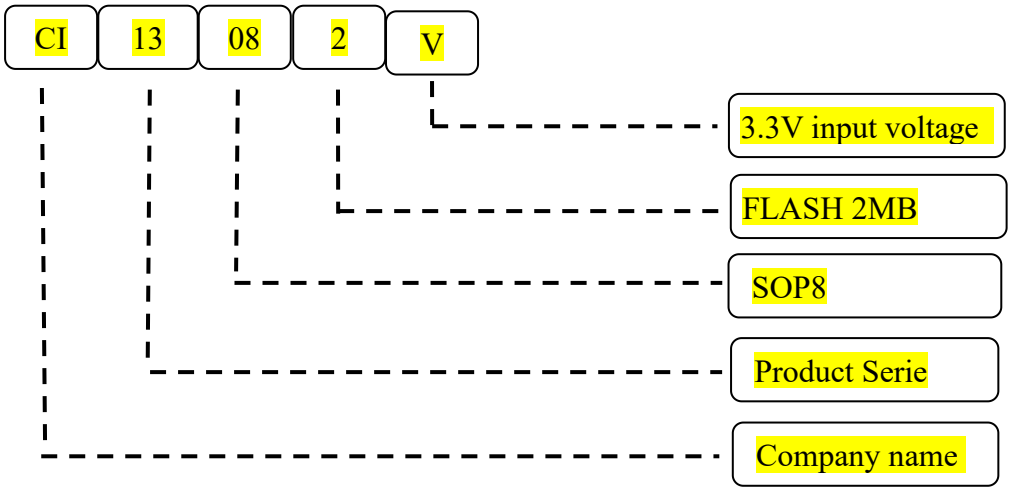


机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	-	-	1.75
A1	0.10	0.15	0.25
A2	1.35	1.45	1.55
b	0.35	-	0.50
c	0.19	-	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	1.27 BSC		
h	0.30	-	0.50
L	0.50	-	0.80
θ	0°	-	8°

5 Order information

The chip package MRAK of CI13082V is shown in the figure below. The first line is the company LOG, the second line is the chip model, the third line is the production batch number, and the dot in the lower left corner is the identification of pin 1.

The chip model is defined as follows:



The order information of CI13082V chip is shown in Table 5-1.

Table 5-1 CI13082V chip order information table

product model	Encapsulation form	Basic packaging	Number of tubes installed	Factory standard package	Standard packing quantity
CI13082V	SOP8	piping and instrumentation	100pcs	box-packed	20000pcs (200 tubes/box)

6 Application

6. 1 Application reference circuit diagram

The CI13082V chip requires minimal peripheral components to develop terminal product solutions supporting various voice applications. This device supports single-microphone single-ended input. Designers can select appropriate circuit designs based on functional requirements, power consumption specifications, and cost considerations for their application solutions.

The following is an example of the typical application scheme of CI13082V to introduce the key points and precautions of application scheme design

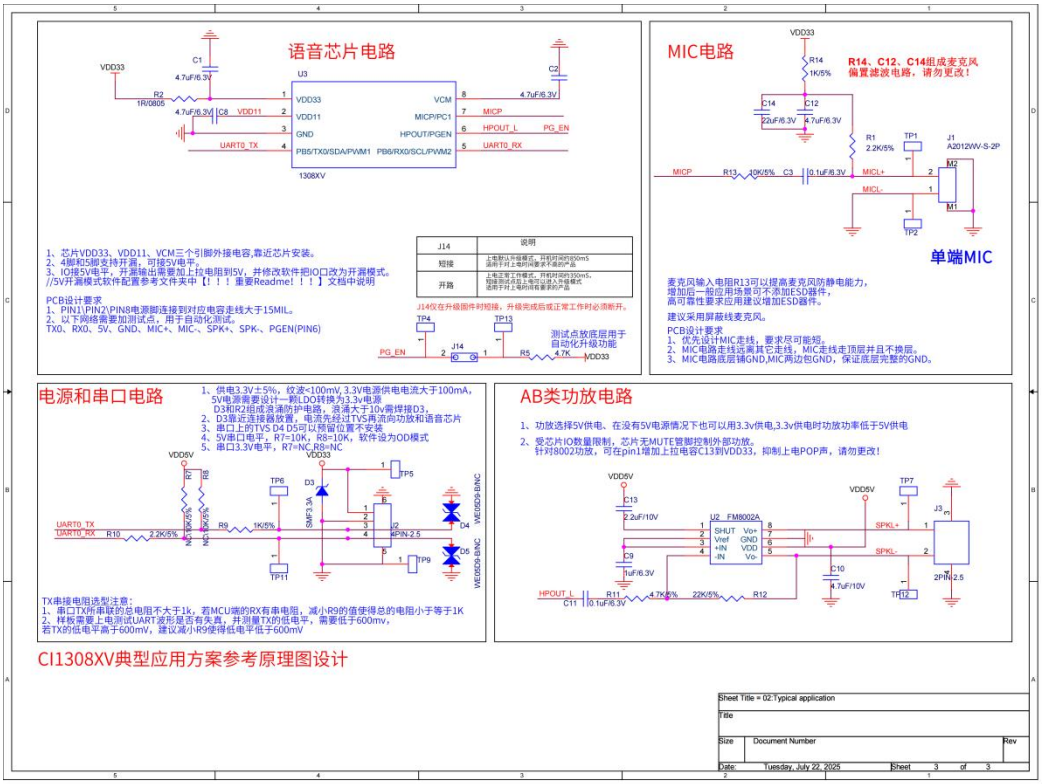


Figure 6-1 Reference circuit diagram of typical application scheme of CI1308XV

The diagram above shows a reference circuit design for a typical application scenario featuring CI13082V and other chips in the CI1308XV series, which uses a single microphone with single-ended input and power amplifier output. This design is not limited to matching any specific end-product. The application design should adhere to the principle of compatibility with host computer terminal products, and reference schematics and PCB layouts can be downloaded from Chipintelli's document center and AI platform based on the functional and performance requirements of the terminal product. Document Center linkhttps://document.chipintelli.com

If the board-level upgrade function needs to be reserved during the application scheme design, UART0 pins can be led out as sockets or test points, so that the firmware can be burned or upgraded through UART0 after the PCB board is soldered.

The CI13082V's HPOUT/PGEN pin is preconfigured with a pull-down resistor on the chip. During power-on, the system checks if this pin is pulled high to 3.3V by an external pull-up resistor. If both conditions are met and an upgrade signal is detected via UART0, the system enters upgrade mode. If no external pull-up resistor is connected to this pin, the system skips the upgrade detection phase and directly enters normal startup mode, enabling rapid boot. For applications requiring fast boot, the HPOUT/PGEN pin can be routed externally with a jumper wire connected to a 4.7KΩ resistor pulling up to VDD33. This configuration enables normal startup mode during power-on, reducing boot time to approximately 350ms. For online upgrades, the PGEN pin can be pulled to 3.3V high voltage by shorting the jumper wire or its test points, allowing UART0-based upgrades. For applications without fast boot requirements, the 4.7KΩ resistor can directly pull up the PGEN pin. Detailed implementation methods should reference the original application diagram or consult our FAE. The two operating modes of PGEN are listed in the table below:

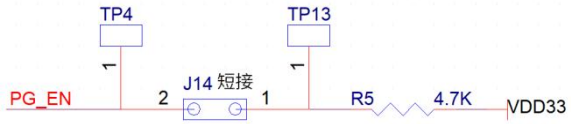
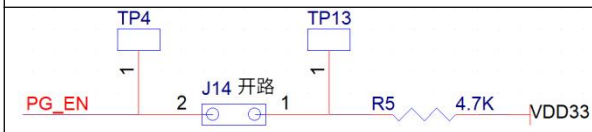
PG_EN working mode diagram	Installation status at J14	PG_EN high and low levels	available machine time
	short circuit	High level, upgrade mode	850ms
	open a way	Low level, working mode	350ms

Table 6-1 CI1308XV Upgrade Mode Table

The CI13082V chip has no MICBIAS foot, and the microphone power supply adopts external 3.3V. It is recommended to use the power supply design in Figure 6-1. The filter circuit composed of R14, C12 and C14 cannot be changed.

CI13082V only supports single microphone input. It is recommended to use the microphone design in Figure 6-1, and the wire length should be less than 20 cm.

The power amplifier configuration of this typical application scheme is AB class power amplifier, and the 8002 series power amplifier is recommended. If the voice broadcast function is not required, the circuit can be removed to reduce the cost of the scheme. The MUTE function of the power amplifier is shown in Figure 6-1.

The UART port of CI13082V supports 5V level communication. If the application scheme requires external 5V communication level, it is recommended to use the serial port design in Figure 6-1. It is only necessary to add a 5V pull-up resistor around the RX and TX pins of UART0, without configuring the level conversion circuit.

Pin 7 of CI13082V is used for microphone and GPIO multiplexing. To use the microphone

input, the internal pull-up of PC1 needs to be closed by software configuration. To use the GPIO, the MIC input needs to be closed by software and configured as high resistance input.

6.2 Other application notes

1. CI13082V is manufactured with lead-free and environmentally friendly materials. When SMT welding, please set furnace temperature and time parameters according to lead-free standards as shown in the figure below

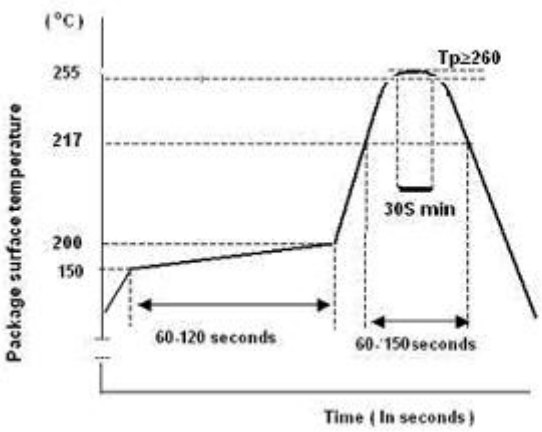


Figure 6-2 Furnace temperature curve

2. Attention should be paid to anti-static measures during the use, handling and production of CI13082V, and its packaging should be made of anti-static materials.

- Chipintelli reserves the right to interpret and modify this specification. If modified, we will not give further notice! Customers should obtain the latest version of the information and verify whether the relevant information is accurate and complete before application design.
- Any semiconductor product may fail or malfunction under certain conditions. The chip application party is responsible for complying with safety standards and taking safety protection measures when using the product for system design and complete machine manufacturing, so as to avoid personal injury or property loss caused by possible product failure!
- Chipintelli will do its best to provide customers with better products and better services!