CI1312 Datasheet

High Performance Automatic Speech Recognition processor

SOP16

Length: 9.9mm
Width: 6.0mm
Thickness: 1.7mm

• Brain Neural Network Processing Unit (BNPU)

– BNPU V3 support DNN \ TDNN \ RNN \ CNN and other neural networks and parallel vector operations. It can realize speech recognition, voiceprint recognition, command word self-learning, voice detection, deep learning noise reduction and other functions

• CPU and Storage

– CPU frequency up to 220 MHz
– 2MBytes of Flash memory inside
– 640K Bytes of SRAM inside
– 512bit eFuse for encryption

• Audio Codec

– High performance, Low-power consumption audio ADC with SNR ≥ 95dB
– Low-power consumption audio DAC with SNR ≥ 95dB

• PWM

– Three PWM interfaces

• GPIO

– 5 fast GPIOs, response speed up to 20MHz
– All GPIOS with 5V input tolerant capability

• Reset and power management

– Build-in PMU
– PMU input voltage range: 3.6V to 5.5V
– Power-on Reset (POR)
– Power Voltage Detector (PVD)

• Clock management

– Built in RC oscillator

• Communication interface

– One IIC interface
– Two UART interfaces with 3M baud rate

• Timer and Watch dog

– Four 32-bit timers, Two watch dogs

Contents

1 Description

1.1 Functional overview

CI1312 is a high-performance artificial intelligence chip for speech recognition and processing. CI1312 integrates brain neural network processor BNPU V3.0 developed by chipintelli , 220Mhz CPU, up to 640k Byte RAM, integrated PMU, integrated RC oscillator, integrated single channel high-performance low-power consumption audio codec, integrated multiple UART, IIC, PWM, GPIO and other peripheral control interfaces, only need a few peripheral device for internal LDO. It has high cost performance.

CI1312 uses industrial design standards and has high environmental reliability. The working temperature range of the chip is between - 40℃ and + 85℃. It complies with MSL3 humidity sensitivity level, 4KV contact discharge test standard of IEC 61000-4-2, FCC electromagnetic compatibility standard and ROHS and REACH environmental protection standards.

CI1312 support the 3rd generation BPNU technology of Chipintelli, which can support support DNN \ TDNN \ RNN \ CNN and other neural networks and parallel vector operations. It can realize speech recognition, voiceprint recognition, command word self-learning, voice detection, deep learning noise reduction and other functions. It also support Chinese, English, Japanese and other global languages.

CI1312 can be widely used by home appliances, lighting, toys, wearable devices, industry, automobile and other product fields to realize voice interaction and control, and the application of various intelligent voice solutions It can implement the requirements of improving efficiency and reducing cost for the existing intelligent speech off-line recognition application.

1.2 Chip Specifications

The functional block diagram of CI1312 chip is shown in the figure below:

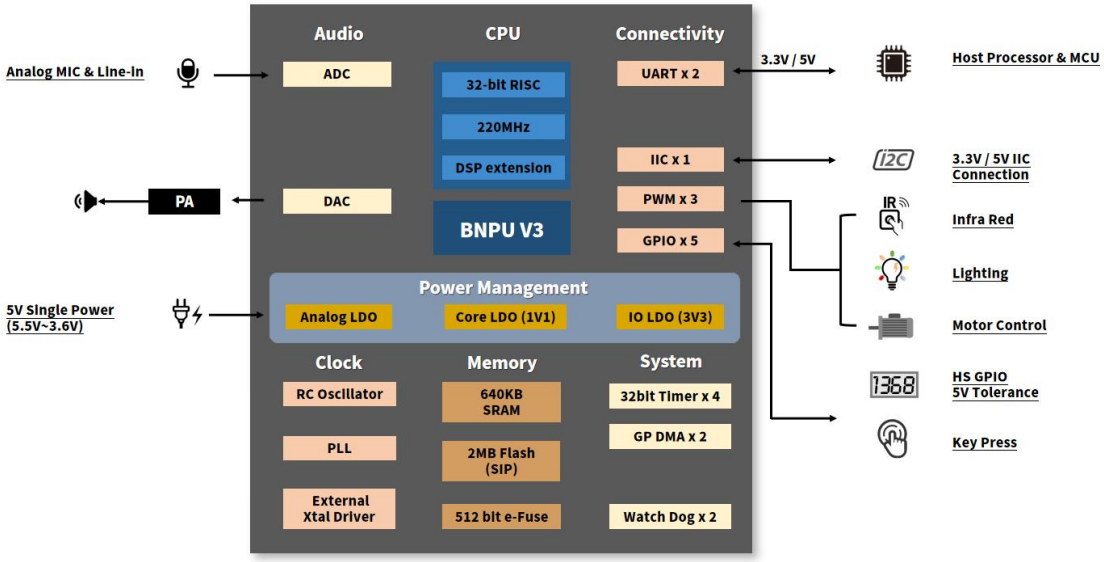


Diagram 1-1 Function Block Diagram

■ **Brain Neural Network Processing Unit（BNPU）**

- BNPU V3 support support DNN \ TDNN \ RNN \ CNN and other neural networks and parallel vector operations. It can realize speech recognition, voiceprint recognition, command word self-learning, voice detection, deep learning noise reduction and other functions

■ **CPU**

- 32 bit high performance CPU, frequency up to 220MHz
- 32 bit signal-period multiplier, support DSP accelerate

■ **Storage**

- 640KB SRAM inside
- 512bit e-Fuse inside
- 2MB Flash inside

■ **Audio Interface**

- High performance, Low consumption audio codec module, support single ADC sampling and signal DAC playing
- Support automatic level control (ALC)
- Support 8kHz/16kHz/24kHz/32kHz/44.1kHz/48kHz Sampling rate

- **PMU**

  - Three LDOs inside, the chip only need a few peripheral device for internal LDOs. External power chip is not necessary

  - 5V Power supply, the power supply range supports a minimum of 3.6V input and a maximum of 5.5V input

- **CLOCK**

  - Built in RC oscillator

- **Peripheral Interface and Timer**

  - Two UART interfaces with 3M baud rate maximum
  - One IIC interface, support IIC extended device
  - Three PWM interfaces, support direct driving for light control and motor applications
  - Four 32-bit timers inside
  - Built-in one independent watchdog（IWDG）
  - Built-in one window watchdog（WWDG）

- **GPIO**

  - Support 5 GPIOS
  - Each GPIOS with 5V tolerant capability. There is no need for external 5V conversion, but the external resistance needs to be pulled up to 5V
  - Each GPIO can be configurable for interruption and support pull up and pull down setting

- **Development Support**

  - Provide software development package, application examples and notices
  - Content and services can be realized online, obtain address: https://platform.chipintelli.com

- **Firmware burning and protection**

  - Support firmware upgrade by UART and firmware protection

- **EMC and ESD**

  - Excellent EMC design and support FCC standard
  - Excellent ESD design, it can pass 4KV contact discharge test

- **ROHS and REACH**

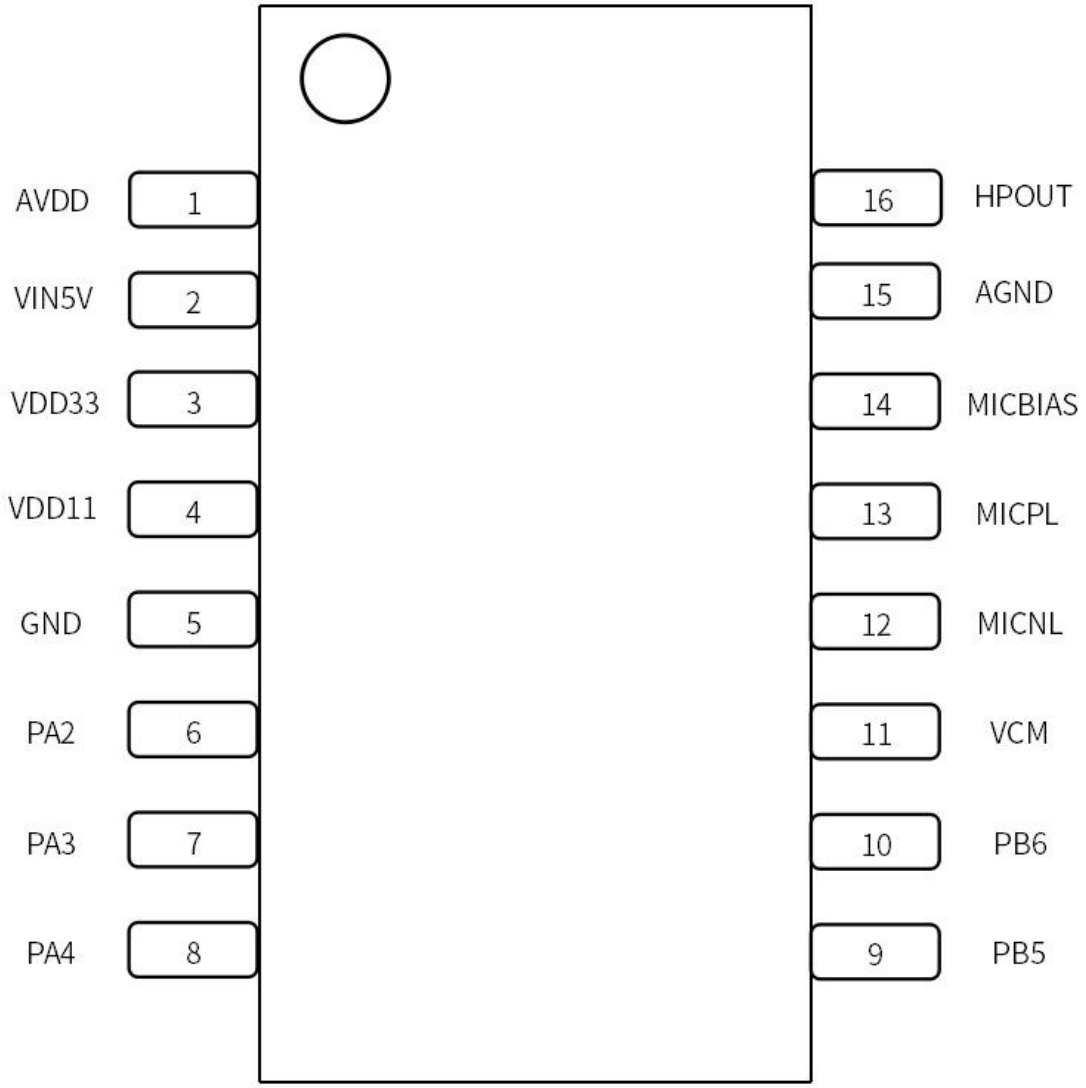
  - Support ROHS and REACH standards

- **Packaging and Operating temperature**

  - Devices Packaging: SOP16, Length*Width*Thickness = 9.9*6.0*1.7 mm
  - Operating temperature: -40℃～+85℃

2 Pin Diagram and Function Description

2.1 Pin Diagram



2.2 Pin descriptions

Table 2-1 Pin Descriptions

Pin number	Pin Name	Type	5V--Tolerant	Power on default state	Description Alternate functions
1	AVDD	P	-	-	3.3V output or 3.3V analog power supply, output capacitance/input capacitance is 4.7uF
2	VIN5V	P	-	-	VIN5V is the PMU power supply input pin. The normal working input voltage range is 3.6V-5.5V. A 4.7uf input capacitor is connected externally. The maximum input voltage of this pin is 6.5V. Note that over-voltage and surge protection devices need to be added, such as a TVS and a 4.7 ohm resistor to protect against surge impact
3	VDD33	P	-	-	3.3V output or 3.3V IO power supply, output capacitance/input capacitance is 4.7uF
4	VDD11	P	-	-	1.1V output or 1.1V Power supply, output capacitance/input capacitance is 4.7uF
5	GND	P	-	-	Ground
6	PA2	IO	√	IN,T+D	1. GPIO PA2 (Initial state at startup) 2. IIC_SDA 3. UART1_TX 4. PWM0
7	PA3	IO	√	IN,T+D	1. GPIO PA3 (Initial state at startup) 2. IIC_SCL 3. UART1_RX1 4. PWM1
8	PA4	IO	√	IN,T+U	1. GPIO PA4 (Initial state at startup)/PG_EN (For software update, Note1) 2. PWM2
9	PB5	IO	√	IN,T+U	1. GPIO PB5 (Initial state at startup) 2. UART0 TX 3. IIC SDA 4. PWM1
10	PB6	IO	√	IN,T+U	1. GPIO PB6 (Initial state at startup) 2. UART0_RX 3. IIC_SCL 4. PWM2
11	VCM	O	-	-	VCM Output
12	MICNL	I	-	-	Left Microphone N input
13	MICPL	I	-	-	Left Microphone P input
14	MICBIAS	O	-	-	Microphone Bias output
15	AGND	P	-	-	Analog ground
16	HPOUT	O	-	-	DAC output

Conformity with definition:

I input

O output

IO bidirectional

P power or ground

T+D Tristate plus pull-down

T+U Tristate plus pull-up

OUT power-on defaults to output mode

IN power-on defaults to input mode

The driving capability of all GPIOs can be configured, and the pull up and pull down resistance can be configured by software.

Note1: At startup, the voltage of Pin PA4(PG_EN) will be detected. When the voltage is high(higher than 2.0V), the chip can start serial port upgrade service and program. When the voltage is low(lower than 0.8V), the chip start directly from Flash as normal.

2.3 Alternate functions

Table 2-2 Alternate Functions

Pin Name	Function1	Function2	Function3	Function4	Function5	Analog Function	Specific Function
PA2	PA2	-	IIC_SDA	UART1_TX	PWM0	-	-
PA3	PA3	-	IIC_SCL	UART1_RX	PWM1	-	-
PA4	PA4	-	-	-	PWM2	-	PG_EN Note1
PB5	PB5	UART0_TX	IIC_SDA	PWM1	-	-	-
PB6	PB6	UART0_RX	IIC_SCL	PWM2	-	-	-

Note1: The PA4(PG_EN) Pin is pulled up by default. When the power on is judged to be high, the chip can automatically enter the upgrade mode when it detects an upgrade signal on UART0 when it is powered on. At this time, the supporting upgrade tool can be used to program the flash inside the chip. If no upgrade signal is detected on UART0, it will enter the normal working mode.

3 Electrical Characteristics

Table 3-1 Electrical Characteristics Table

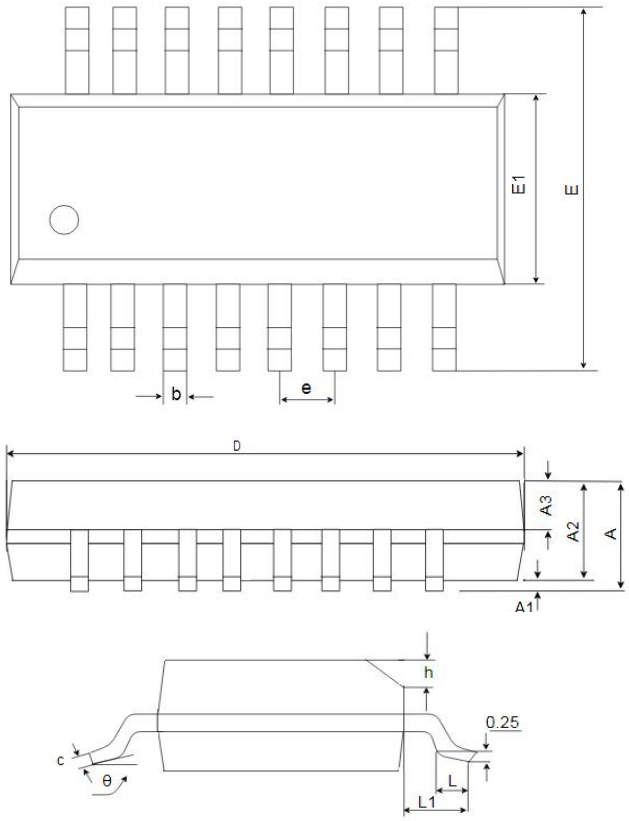
Symbol	Description	Min.	Typical	Max.	Unit
VIN5V	PMU Power supply	3.6	5	5.5	V
AVDD	Analog Codec Power supply	2.97	3.3	3.63	V
VDD33	Chip IO Power Supply	2.97	3.3	3.63	V
VDD11	Chip core Power Supply Voltage	0.99	1.1	1.22	V
V_{IH}	Input High Voltage, 3.0V ≤ VDD33 ≤ 3.6V	0.7×VDD33	-	-	V
V_{IL}	Input Low Voltage, 3.0V ≤ VDD33 ≤ 3.6V	-	-	0.3×VDD33	V
V_{OL}	Output Low Voltage @I_{OL} = 2,4mA	-	-	0.4	V
V_{OH}	Output High Voltage @I_{OH} = 2,4mA	2.4	-	-	V
I_{5VIO}	Driving current when IO (withstand 5V voltage) outputs 3.3V	5	-	23	mA
I_{33VIO}	Driving current when IO (withstand 3.3V voltage) outputs 3.3V	12	-	26	mA
ΣIVDD	Driving current of all GPIOs	-	-	180	mA
Pde	5V power supply, and the chip's VDD11 is powered by external DC-DC chip. The total power consumption of 5V input during normal identification at TA= 25°C	70	-	150	mW
Pdi	5V power supply, and the chip uses internal PMU. The total power consumption of 5V input during normal identification at TA= 25°C	145	-	250	mW
RC Oscillator Accuracy Note1	T_A=-20 to 85°C	-3	-	+3	%
	T_A=-10 to 70°C	-2.5	-	+2.5	%
T_A Note2 Note3	Working ambient temperature that the chip using internal RC oscillator can adapt to	-10	-	+70	℃
T_{ST}	Chip Storage temperature	-55	-	+150	℃

Note1: The RC oscillator built in the chip will produce a certain temperature drift with the change of the ambient temperature. This temperature drift may affect the application requiring high-precision clock or the accuracy of serial communication with upper computer.

Note2: The application uses the internal RC oscillator as the clock source, and the baud rate of serial communication must be less than or equal to 115200bps. At the same time, the total deviation between the baud rate and the serial port of the upper computer shall not exceed 4% to ensure good communication. If the working environment temperature is - 10 to 70 ℃, the baud rate deviation of the serial port of the upper computer must not exceed ± 1.5% in this temperature range. If the working environment temperature is - 20 to 85 ℃, the baud rate deviation of the serial port of the upper computer must not exceed ± 1% in this temperature range.

Note3: When the upper computer is designed without crystal oscillator, the communication error should be minimized. Chipintelli can provide a self-adaptive scheme for baud rate of serial port, which needs to add a handshake command to the serial port protocol, and the upper computer ensures that it will reply according to the protocol requirements within 50ms after receiving the handshake command. After adding this self-adaptive scheme, the product can be used in applications where the working environment temperature is - 20 to 85 ℃.

4 Packaging Information



COMMON DIMENSIONS

SYMBOL	UNIT：MILLIMETER		
	MIN	NOM	MAX
A	_	_	1.70
A1	0.10	_	0.225
A2	1.30	1.40	1.50
A3	0.6	0.65	0.70
b	0.39	_	0.47
c	0.20	_	0.24
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	_	0.50
L	0.50	0.6	0.80
L1	1.05REF		
θ	0	_	8°

5 Order Information

Table 5-1 Order Information Table

Orderable Device	Flash	Status	Package Type	Pins	Package Qty	Eco Plan	MSL Peak Temp	Op Temp (℃)
CI1312	2MByte	MP	SOP16/Tube	16	50	RoHS & Green	Level-3 260C-UNLIM	-40 to 85

6 Application

6.1 Application Reference Circuit Diagram

The periphery of CI1312 chip only needs a few devices to support all kinds of voice applications. The chip can support single microphone differential input or single microphone single ended input. Users can select the appropriate circuit according to the function, power consumption and cost requirements of the designed application scheme. The simplest application reference circuit diagram of the chip is described in detail below.

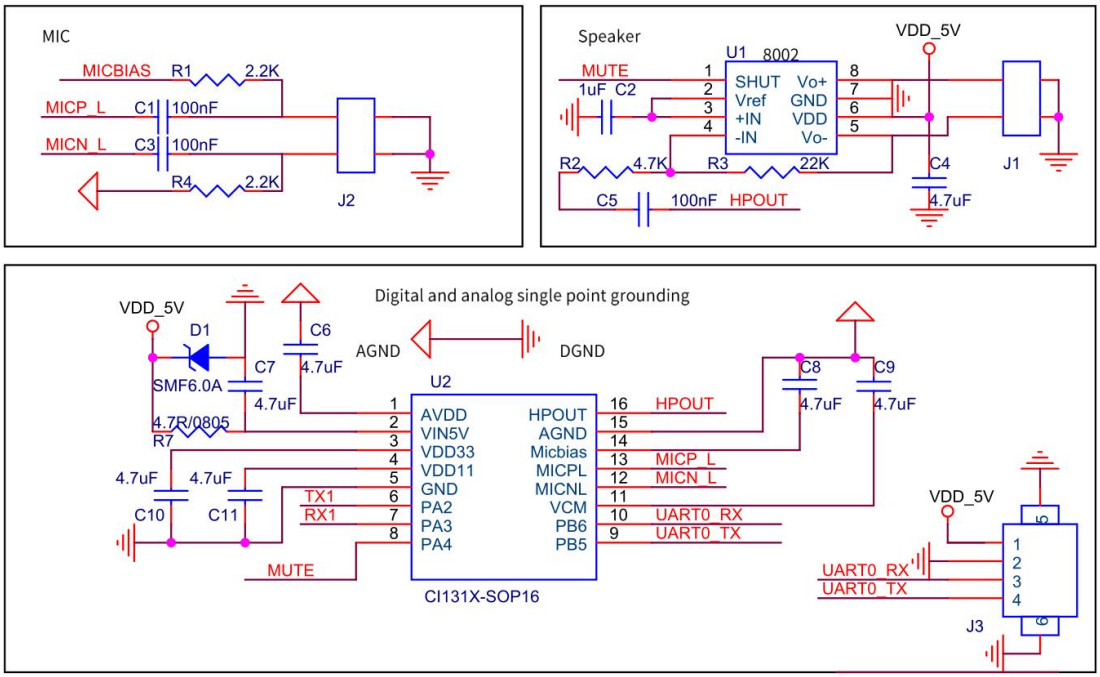


Diagram 6-1 The circuit diagram of the simplest CI1312's application scheme

The figure above is the circuit diagram of the simplest CI1312's application scheme, supporting single microphone differential input and power amplifier output. The chip can use 5V direct power supply, and users can design according to the corresponding peripheral device specifications in the figure above.

If the online upgrade function is to be considered in the schematic design, the UART0 pin can be led out, to facilitate the firmware upgrade of the flash inside the main chip through UART0. The PA4 (PG_EN) pin of the chip is internally pulled up, and the power on defaults state is the upgrade mode. After power on, the chip detect the upgrade signal from the external UART0 port, and directly start the upgrade. The default startup time of the chip is about 850ms with extending due to the detection of upgrade mode. If the user has high requirements for the startup time, the PA4 pin can be led out, two 2.2kΩ pull-down resistors can be added to the ground, and a test point is added in the middle of the two 2.2kΩ resistors. At this time, the chip's startup state is in the

normal mode, and the startup time is about 350ms, which can shorten the startup time. If you want to upgrade online at this time, you can supply high level to the intermediate test points connected by two 2.2kΩ resistors externally, pull PA4 pin up, and then upgrade through UART0.

The chip scheme can choose differential microphone design or single ended microphone design. The differential microphone design in the figure above is recommended. If the user has requirements to reduce the cost, the microphone part in the figure above can be modified to the single ended microphone design, which can use less passive devices than the differential microphone. However, this method is only recommended to be used when the microphone line length is less than 20cm. Otherwise, because the line is too long and the anti-interference effect is not enough, the speech recognition effect is not as good as that of the differential microphone design. The power amplifier in the figure above adopts class AB power amplifier, and 8002 power amplifier chip is recommended. Users can also choose the power amplifier chip according to the requirements of the scheme. If the power amplifier function is not required, this part of the circuit can also be removed to reduce the cost.

If the user has no special requirements to reduce the power consumption, it is recommended to directly use the PMU inside the chip for power supply. If there are requirements to reduce the power consumption, an external DCDC chip can be added to supply power to the chip at 1.1V to reduce power consumption. The UART ports of the chip support 5V communication. The UART0 port in the figure above is connected with a 3.3V signal. If 5V is to be connected, add a pull-up resistance connected to 5V around the RX and TX pins of UART0 without adding an additional voltage conversion circuit.

6.2 Other Application Notices

1. Due to the principle of semiconductor technology, the RC oscillator built in the chip will produce certain temperature drift in high-temperature and low-temperature environments. If the operating temperature range of the application is -10 to 70 ℃, and only low-speed serial port communication (baud rate less than or equal to 115200bps) is conducted with the upper computer, this kind of circuit scheme can use the RC oscillator built in the chip(the frequency deviation of upper computer must be equal to or less than ± 1.5%). When the upper computer is designed without crystal oscillator, the communication error should be minimized. Chipintelli can provide a self-adaptive scheme for baud rate of serial port, which needs to add a handshake command to the serial port protocol, and the upper computer ensures that it will reply according to the protocol requirements within 50ms after receiving the handshake command. After adding this self-adaptive scheme, the product can be used in applications where the working environment temperature is -20 to 85 ℃.

2. If the application requires a temperature range of - 40 to 85 ℃, please use CI130x series chips and external crystal oscillators.

3. The PMU in the chip include three LDOs, The LDOs provide 3.3V and 1.1V for chip Operating. In general, external power chips for 3.3V and 1.1V Power supply is not necessary. The ripple of external 5V power supply shall be less than 300mV.

4. The chip is lead-free. When SMT soldering, please set parameters such as furnace temperature and time according to lead-free standard.

5. We should pay attention to the electrostatic effect when we use and pack chips. It is suggested that antistatic materials be used for isolation.