CI13162 Datasheet

High Cost Performance Automatic Speech Recognition Chip

• Brain Neural Network Processing Unit (BNPU)

– BNPU V3.5 support DNN \ TDNN \ RNN \ CNN and other neural networks and parallel vector operations. It can realize speech recognition, call noise reduction

• CPU and Storage

– CPU frequency up to 210 MHz

– 2 MBytes of Flash memory inside

– 288 KBytes of SRAM inside

– 256 bit eFuse for encryption

• Audio Codec

– High performance, Low-power consumption audio ADC with SNR ≥ 95dB

– Low-power consumption audio DAC with SNR ≥ 95dB

• PWM

– Three PWM interfaces

• GPIO

– 6 fast GPIOs, response speed up to 20MHz

– 5 GPIOS with 5V input tolerant capability

• Reset and power management

– Build-in PMU

– PMU input voltage range: 3.6V to 5.5V

– Power-on Reset (POR)

– Power Voltage Detector (PVD)

• Clock management

– Built in RC oscillator

– Support external crystal oscillator input

• Communication interface

– One IIC interface

–Two UART interfaces with 5V input tolerant capability ， with 3Mbps baud rate

• Timer and Watch dog

– Two 32-bit timers, One watch dogs

Contents

1 Description

1.1 Functional overview

CI13162 is a high-performance artificial intelligence chip for speech recognition and processing. CI13162 integrates brain neural network processor BNPU V3.5 developed by chipintelli , 210Mhz CPU, up to 288 KByte SRAM, integrated PMU, integrated RC oscillator, integrated single channel high-performance low-power consumption audio codec, integrated multiple UART, IIC, PWM, GPIO and other peripheral control interfaces, only need a few peripheral device for internal LDO. It has high cost performance.

CI13162 uses industrial design standards and has high environmental reliability. The working temperature range of the chip is between - 40℃ and + 85℃. It complies with MSL3 humidity sensitivity level, 4KV contact discharge test standard of IEC 61000-4-2, ROHS and REACH environmental protection standards.

CI13162 adopt the new generation BNPU technology of Chipintelli, which can support DNN \ TDNN \ RNN \ CNN and other neural networks and parallel vector operations. It can realize speech recognition, call noise reduction. It also support Chinese, English, Japanese and other global languages. can be widely used by home appliances, lighting, toys, wearable devices, industry, automobile and other product fields to realize voice interaction and control, and the application of various intelligent voice solutions It can implement the requirements of improving efficiency and reducing cost for the existing intelligent speech off-line recognition application.

1.2 Chip Specifications

The functional block diagram of CI13162 chip is shown in the figure below:

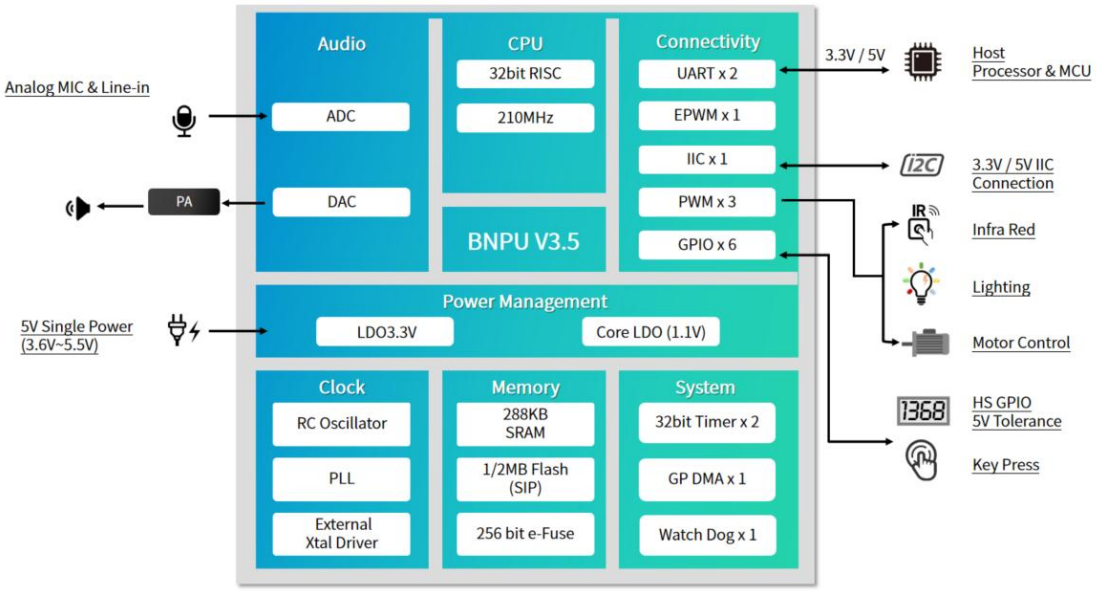


Figure 1-1 CI13162 Function Block Diagram

■ **Brain Neural Network Processing Unit（BNPU）V3.5**

- BNPU V3.5 support DNN \ TDNN \ RNN \ CNN and other neural networks and parallel vector operations. It can realize speech recognition, call noise reduction

■ **CPU**

- 32 bit high performance CPU, frequency up to 210 MHz

■ **Storage**

- 288KB SRAM inside
- 256bit e-Fuse inside
- 2MB Flash inside

■ **Audio Interface**

- High performance, Low consumption audio codec module, support single ADC sampling and signal DAC playing
- Support automatic level control (ALC)
- Support 8kHz/16kHz/24kHz/32kHz/44.1kHz/48kHz Sampling rate

■ **PMU**

- Supports wide power supply voltage, with a power supply range of 3.6V to 5.5V
- Built in 2 high-performance LDO circuits, no need to configure external power chips, application solutions only require a small number of peripheral resistive and capacitive devices

- **CLOCK**

  - Built in RC oscillator

  - Support external crystal oscillator input

- **Peripheral Interface and Timer**

  - Two UART interfaces with 3M baud rate maximum
  - One IIC interface, support IIC extended device
  - Three PWM interfaces, support direct driving for light control and motor applications
  - Two 32-bit timers inside
  - Built-in one independent watchdog（IWDG）

- **GPIO**

  - Support 6 GPIOS, Can be used as the main control IC application
  - Each GPIOS with 5V tolerant capability. There is no need for external 5V conversion, but the external resistance needs to be pulled up to 5V
  - Each GPIO can be configurable for interruption and support pull up and pull down setting

- **Development Support**

  - Provide software development package, application examples and notices
  - Content and services can be realized online, obtain address: https://aiplatform.chipintelli.com

- **Firmware burning and protection**

  - Support firmware upgrade by UART and firmware protection

- **ESD**

  - Excellent ESD design, it can pass 4KV contact discharge test

- **ROHS and REACH**

  - Support ROHS and REACH standards

- **Packaging and Operating temperature**

  - Devices Packaging: SOP16, Length*Width*Thickness = 9.9*6.0*1.7 mm
  - Operating temperature: -40℃～+85℃

2 Pin Diagram and Function Description

2.1 Pin Diagram

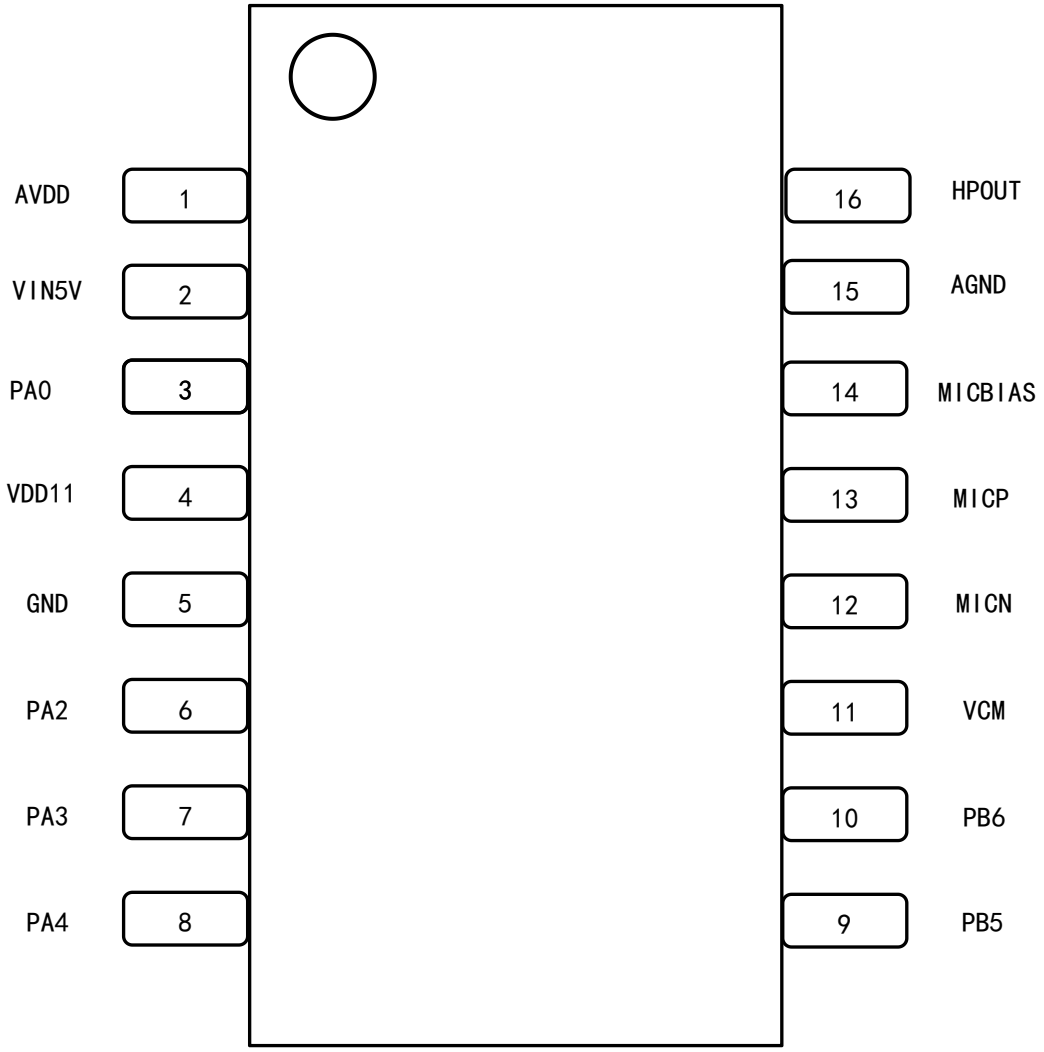


Figure 2-1 CI13162 Pin Sequence and Definition Diagram

2.2 Pin descriptions

Table 2-1 Pin Descriptions

Pin number	Pin Name	Type	5V--Tolerant	Power on default state	Description Alternate functions
1	AVDD	P	-	-	● Internal LDO-3.3V output ● Internal analog circuit 3.3V power supply input * Note1*
2	VIN5V	P	-	-	● Power supply voltage range 3.6V to 5.5V * Note1*
3	PAO	IO	-	-	● XIN（Initial state at startup) ● GPIO PA0 ● PWM2

4	VDD11	P	-	-	● LDO-1.1V output ● Core 1.1V power input * Note1*
5	GND	P	-	-	Ground
6	PA2	IO	√	IN,T+D	● GPIO PA3 (Initial state at startup) ● IIC_SDA ● UART1_TX ● PWM0 ● PWMP
7	PA3	IO	√	IN,T+D	● GPIO PA3 (Initial state at startup) ● IIC_SCL ● UART1_RX1 ● PWM1 ● PWMN
8	PA4	IO	√	IN,T+U	● GPIO PA4 (Initial state at startup)/PG_EN * Note2* ● PWM2
9	PB5	IO	√	IN,T+U	● GPIO PB5 (Initial state at startup) ● UART0_TX ● IIC_SDA ● PWM1 ● PWMP
10	PB6	IO	√	IN,T+U	● GPIO PB6 (Initial state at startup) ● UART0_RX ● IIC_SCL ● PWM2 ● PWMN
11	VCM	O	-	-	VCM POWER Output
12	MICN	I	-	-	Microphone N input
13	MICP	I	-	-	Microphone P input
14	MICBIAS	O	-	-	Microphone bias output
15	AGND	P	-	-	Analog ground
16	HPOUT	O	-	-	DAC output

* Note1* The pins need to be externally connected to a 4.7uF capacitor

* Note2* When powered on, the pin is at a high level, and the system will enter programming mode

Conformity with definition:

I input

O output

IO bidirectional

P power or ground

T+D Tristate plus pull-down

T+U Tristate plus pull-up

OUT power-on defaults to output mode

IN power-on defaults to input mode

The driving capability of all GPIOs can be configured, and the pull up and pull down resistance can be configured by software.

2.3 Alternate functions

Table 2-2 Alternate Functions

Pin Name	Function1	Function2	Function3	Function4	Function5	Function6	Specific Function
PA0	PA0	PWM2					XIN
PA2	PA2	-	IIC_SDA	UART1_TX	PWM0	PWMP	
PA3	PA3	-	IIC_SCL	UART1_RX	PWM1	PWMN	
PA4	PA4	-	-	-	PWM2		PG_EN *Note1*
PB5	PB5	UART0_TX	IIC_SDA	PWM1	PWMP		
PB6	PB6	UART0_RX	IIC_SCL	PWM2	PWMN		

Note1: The PA4 (PG-EN) pin is pulled up by default internally. When the system detects that the pin is at a high level and there is a firmware upgrade signal on the UART0 interface when powered on, it automatically enters the upgrade mode. At this time, the internal Flash of the chip can be programmed using the upgrade tool. If the system does not detect a firmware upgrade signal on the UART0 interface or detects a low voltage on the PA4 pin at this time, it will enter normal working mode.

3 Electrical Characteristics

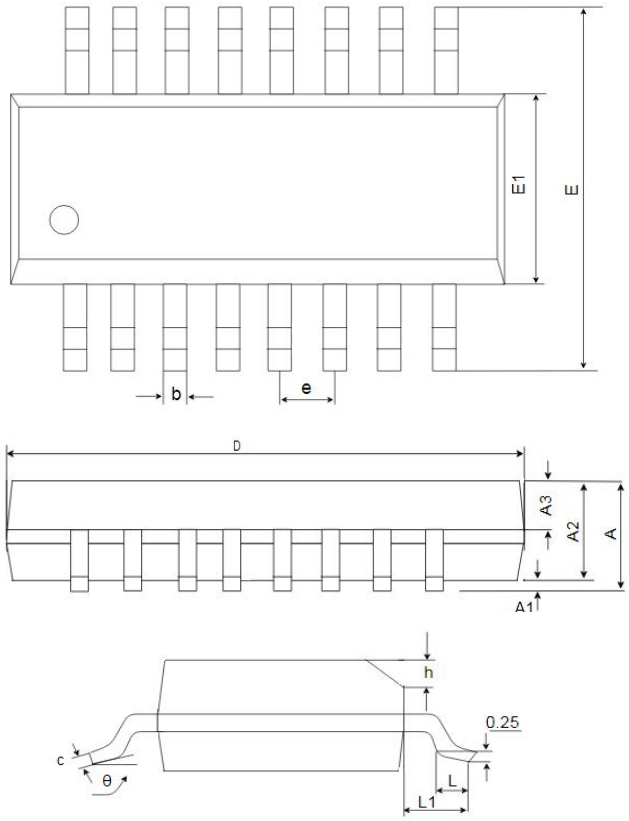
Table 3-1 Electrical Characteristics Table

Symbol	Description	Min.	Typical	Max.	Unit
VIN5V	Chip power supply *Note1*	3.6	5.0	5.5	V
AVDD	3.3V power	2.97	3.3	3.63	V
VDD11	1.1V power	0.99	1.1	1.21	V
V_{IH}	Input High Voltage（3.0V ≤VDD33 ≤ 3.6V）	0.7×VDD33	-	VDD33+0.3	V
V_{IL}	Input Low Voltage（3.0V ≤ VDD33 ≤ 3.6V）	-0.3	-	0.3×VDD33	V
V_{OL}	Output Low Voltage @I_{OL} = 12mA	-	-	0.4	V
V_{OH}	Output High Voltage @I_{OH} = 20mA	2.4	-	-	V
I5V-IO	Driving current when IO (withstand 5V voltage) outputs 3.3V	20	-	33	mA
I3V3-IO	Driving current when IO (withstand 3.3V voltage) outputs 3.3V	14	-	24	mA
ΣIVDD	Driving current of all IO	-	-	200	mA
Pde	5V power supply, and the chip's VDD11 is powered by external DC-DC chip. The total power consumption of 5V input during normal identification at TA= 25°C	40	-	90	mW
Pdi	5V power supply, and the chip uses internal PMU. The total power consumption of 5V input during normal identification at TA= 25°C	125	-	255	mW
RC Oscillator Accuracy *Note2*	TA：-40℃～+85℃	-1.5	-	+1.5	%
Top	Chip working environment temperature	-40	-	+85	℃
Tst	Chip storage environment temperature	-55	-	+150	℃

Note1: Require ripple to be less than 300mVp-p.

Note2: Due to the principles and characteristics of semiconductor technology, the built-in RC oscillator of the chip will produce a certain temperature drift (± 1.5%) in its oscillation frequency accuracy in high and low temperature environments. CI13162 has a built-in baud rate adaptive circuit, which can support normal communication between the chip and the upper computer in high and low temperature environments. If the application plan requires the clock of the chip to be very accurate, please use a chip equipped with an external crystal oscillator and corresponding application plan from chipintelli.

4 Packaging Information



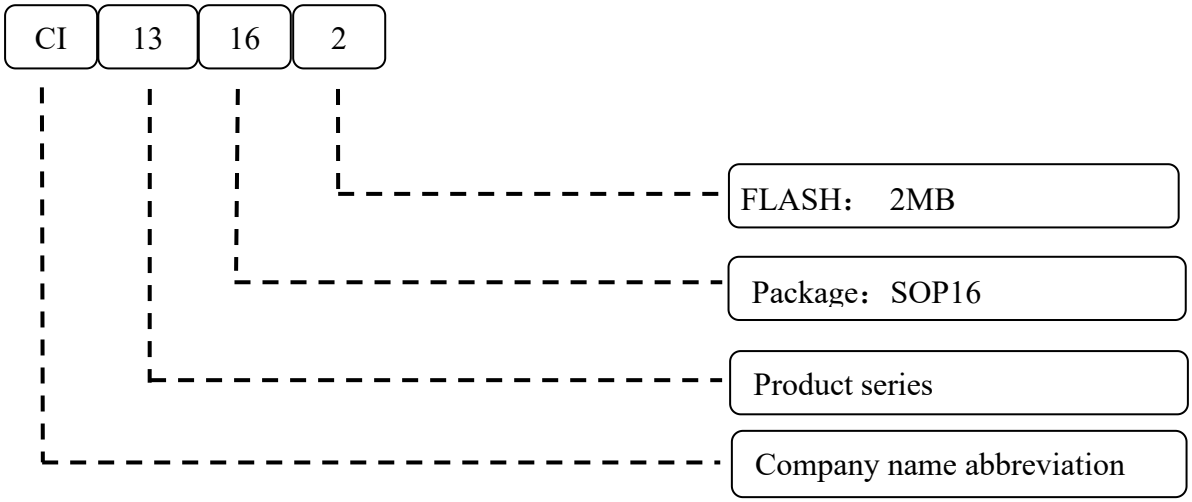
COMMON DIMENSIONS

SYMBOL	UNIT：MILLIMETER		
	MIN	NOM	MAX
A	_	_	1.70
A1	0.10	_	0.225
A2	1.30	1.40	1.50
A3	0.6	0.65	0.70
b	0.39	_	0.47
c	0.20	_	0.24
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	_	0.50
L	0.50	0.6	0.80
L1	1.05REF		
θ	0	_	8°

5 Order Information

The MRAK for CI13162 chip packaging is shown in the following figure. The first line is the company logo, the second line is the chip model, and the third line is the production batch number. The dot in the bottom left corner is the 1-pin identifier.

The definition of chip model is as follows:



The ordering information of CI13162 chip is shown in Table 5-1.

Table 5-1 Order Information Table

Chip model	Package Type	Basic packaging	Package Qty	Ex-factory packaging	Standard Pack Qty
CI13162	SOP16	Pipe installation	50pcs	box-packed	10000pcs （200 tubes/box）

6 Application

6.1 Application Reference Circuit Diagram

The CI13162 chip only requires a small number of peripheral components to develop terminal product solutions that support various voice applications. CI13162 supports single microphone differential or single ended input. Application scheme design can select a suitable circuit design scheme based on the required factors such as functionality, power consumption, and cost.

Taking the typical application scheme of CI13162 as an example, the key points and precautions of application scheme design are introduced below

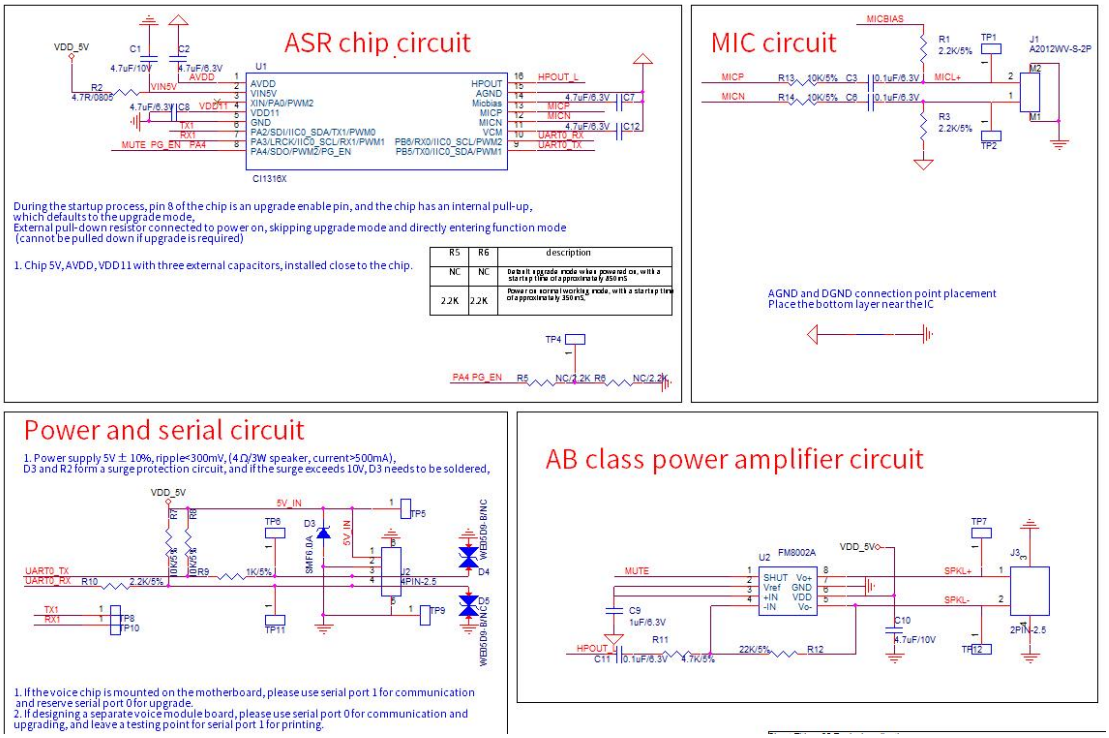


Figure 6-1 The circuit diagram of the simplest CI13162's application scheme

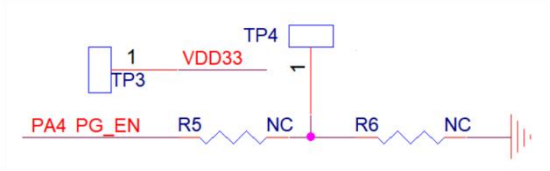
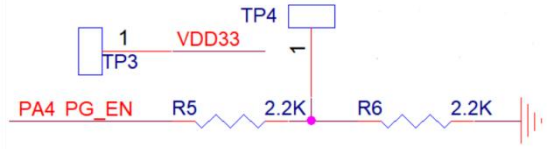
The above diagram is a reference design circuit diagram for typical application scenarios of CI1316X series chips, including CI13162, with single microphone differential input and power amplifier output. This design is not limited to matching a specific terminal product. The design of application solutions should be based on the principle of adapting to upper computer terminal products, and according to the functional and performance requirements of the terminal products, go to the chipintelli document center and AI platform to download reference schematics and reference PCB diagrams. Document Center Link https://document.chipintelli.com/

If a board level upgrade function needs to be reserved during application design, the UART0 pin can be led out in the form of a socket or test point, so that the PCB board can be burned or

firmware can be upgraded through UART0 after SMT is completed.

The PA4 (PG-EN) pin of CI13162 has a preset 3.3V pull-up resistor inside the chip. When powered on, the system will detect whether the pin is set to a high level of 3.3V. If it is high and the UART0 pin is detected to have an external input upgrade signal, the system will enter upgrade mode. If the pin is externally connected with a pull-down resistor to ground, the chip can skip the upgrade mode detection step and directly enter normal startup mode when powered on, in order to achieve rapid system startup. If there is a need for fast startup in the application solution, PA4 pin can be led out and two 2.2K Ω pull-down resistors can be connected in series to the ground. A test point should be reserved between the two 2.2K Ω resistors (please refer to the original application diagram or consult our company's FAE for specific implementation plans). The two working modes of PG-EN are shown in the table below.

Table 6-1 CI1316X Upgrade Mode Table

PG_EN External Resistance Diagram	R5\R6 Installation	PG_EN High and low levels	Turn on Time
	R5\R6 NC	High level, upgrade mode	850ms
	R5\R6 sticker 2.2K	Low level, working mode	350ms

CI13162 supports differential microphone input or single ended microphone input, and it is recommended to use the differential microphone design shown in Figure 6-1. Low cost design solutions can adopt a single ended microphone input design to reduce the number of components on the microphone input line, but this method is only recommended for solutions with microphone input line lengths less than 20 centimeters. Otherwise, the microphone input line being too long will affect its anti-interference ability, leading to poor speech recognition performance.

The amplifier configuration for this typical application scheme is AB class amplifier, and it is recommended to use 8002 series amplifiers. If voice broadcasting function is not required, this part of the circuit can be removed to reduce the cost of the solution.

If the application solution does not require ultra-low power consumption, it is recommended to use the internal PMU power supply of CI13162 in the design scheme to reduce costs. If the application solution requires ultra-low power consumption, an external DCDC circuit can be used to supply 1.1V power to CI13162 to reduce system power consumption.

The UART port of CI13162 can support 5V level communication. The UART0 port in the above figure is based on a 3.3V communication level as an example. If an application solution requires an external 5V communication level, adding a 5V pull-up resistor around the RX and TX pins of UART0 is sufficient, without the need to configure a level conversion circuit.

6.2 Other Application Notices

1. CI13162 is made of lead-free environmentally friendly materials. When SMT welding, please set the furnace temperature and time parameters according to lead-free standards. As shown in the following figure

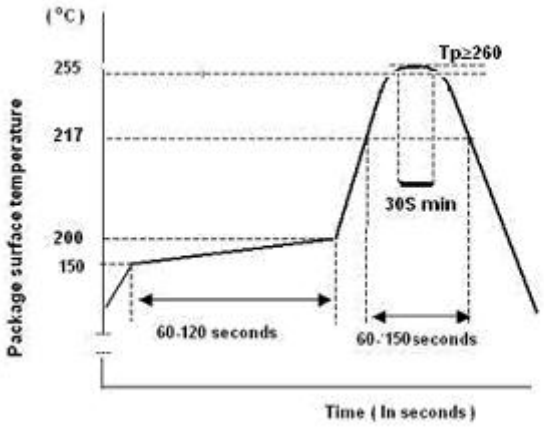


Figure 6-2 Furnace Temperature Curve

2. The use, handling, production and processing of CI13162 require attention to anti-static measures, and its packaging should use anti-static materials.

- Chipintelli reserves the right to change the instruction without further notice. Customers should obtain the latest version before placing an order, and verify that the relevant information is complete and up-to-date.
- Under specific conditions, any semiconductor product has a certain possibility of failure or failure. The buyer has the responsibility to comply with safety standards and take safety measures when using the product for system design and manufacturing, to avoid potential failure risk which may cause personal injury or property loss.
- Product improvement is endless. Chipintelli will provide customers with better products wholeheartedly!