CI230X Datasheet

High Performance ASR Offline/Online Processor

QFN40

Length: 7.0mm
Width: 7.0mm
Thickness: 0.85mm

• WIFI

– Single frequency 2.4GHz IEEE 802.11b/g/n

– Support STA/AP/STA+AP mode

– Integrated protocol stack: TCP/UDP/HTTP/HTTPS/PING/MQTT TLS support for TCP/UDP/HTTP

• BLE

– Support Bluetooth LE 5.1

– Support long range (125Kbps, 500Kbps) and high transmission rate (2Mbps)

• Brain Neural Network Processing Unit (BNPU)

– BNPU V3 support DNN \ TDNN \ RNN \ CNN and other neural networks and parallel vector operations. It can realize speech recognition, voiceprint recognition, command word self-learning, voice detection, deep learning noise reduction and other functions

• CPU and Storage

– CPU frequency up to 220 MHz

– 4/6 MBytes of Flash memory inside

– Built in large capacity SRAM

• Audio Codec

– High performance, Low-power consumption audio ADC with SNR ≥ 95dB

– Low-power consumption audio DAC with SNR ≥ 95dB

• Audio interfaces

– One IIS interface, master/slave configurable

– One Dual-channel PDM interface

• ADC and PWM

– Two channel 12bit SAR ADC

– Six PWM interfaces

• GPIO

– 33 fast GPIOS, response speed up to 20MHz

– 14 GPIOS with 5V input tolerant capability

• Reset and power management

– Build-in PMU

– PMU input voltage range: 3.6V to 5.5V

– Power-on Reset (POR)

– Power Voltage Detector (PVD)

• Communication interface

– One IIC interface

– Two UART interfaces, supporting 5V communication and maximum 3Mbps rate

• Timer and Watch dog

– Four 32-bit timers, Two watch dogs

Catalogue

1 Description

1.1 Functional overview

CI230X is a high-performance artificial intelligence chip for speech recognition and processing. CI230X integrates brain neural network processor BNPU V3.0 developed by chipintelli, and support the combo function of WIFI and BLE. The main frequency of the system can reach 220MHz, and built in a large capacity SRAM, PMU, integrated dual channel high-performance low-power consumption audio codec, integrated multiple UART, IIC, IIS, PWM, GPIO, PDM and other peripheral control interfaces. The chip supports 2.4GHz 802.11 b/g/n WIFI and BLE 5.1 wireless communication protocols. Only a few peripheral components such as resistors and capacitors are needed to realize various hardware solutions for intelligent voice offline+online products, which is very cost-effective.

CI230X uses industrial design standards and has high environmental reliability. The working temperature range of the chip is between - 40 ℃ and + 85 ℃. It complies with MSL3 humidity sensitivity level, 4KV contact discharge test standard of IEC 61000-4-2, FCC electromagnetic compatibility standard and ROHS and REACH environmental protection standards.

CI230X support the 3rd generation BPNU technology of Chipintelli, which can support support support DNN \ TDNN \ RNN \ CNN and other neural networks and parallel vector operations. It can realize speech recognition, voiceprint recognition, command word self-learning, voice detection, deep learning noise reduction and other functions. The effect of it's speech recognition is better than other speech chips. It also support Chinese, English, Japanese and other global languages.

CI230X can be widely used by home appliances, lighting, toys, wearable devices, industry, automobile and other product fields to realize voice interaction and control, and the application of various intelligent voice solutions It can implement the requirements of improving efficiency and reducing cost for the existing intelligent speech off-line recognition application.

At present, CI230X includes CI2305 and CI2306. The pins of these two chips are fully compatible, and only the built-in Flash capacity is different. The CI2305 has 4MB Flash and the CI2306 has 6MB Flash. Due to the small Flash capacity, CI2305 only supports offline speech recognition and IOT connected for AIOT applications. CI2306 can support offline+online speech recognition, and supports larger capacity neural network models and more sound playback, with better noise reduction effect.

1.2 Chip Specifications

■ **WIFI**

- Single frequency 2.4GHz IEEE 802.11b/g/n
- Support STA/AP/STA+AP mode
- Integrated protocol stack: TCP/UDP/HTTP/HTTPS/PING/MQTT, TLS support for TCP/UDP/HTTP
- Integrated PA/LNA/TRX Switch

■ **BLE**

- Support Bluetooth LE 5.1
- Support long range (125Kbps, 500Kbps) and high transmission rate (2Mbps)

■ **Brain Neural Network Processing Unit(BNPU)**

- BNPU V3 support support DNN \ TDNN \ RNN \ CNN and other neural networks and parallel vector operations. It can realize speech recognition, voiceprint recognition, command word self-learning, voice detection, deep learning noise reduction and other functions

■ **CPU**

- 32 bit high performance CPU, frequency up to 220MHz
- 32 bit signal-period multiplier, support DSP accelerate

■ **Storage**

- Large capacity SRAM inside
- 512bit e-Fuse inside
- 4/6MB Flash inside

■ **Audio Interface**

- High performance, Low consumption audio codec module, support double ADC sampling and signal DAC playing
- Support automatic level control (ALC)
- Support 8kHz/16kHz/24kHz/32kHz/44.1kHz/48kHz Sampling rate
- Support one IIS audio extended path
- Support one PDM interface, it can support one or two digital MEMS microphone

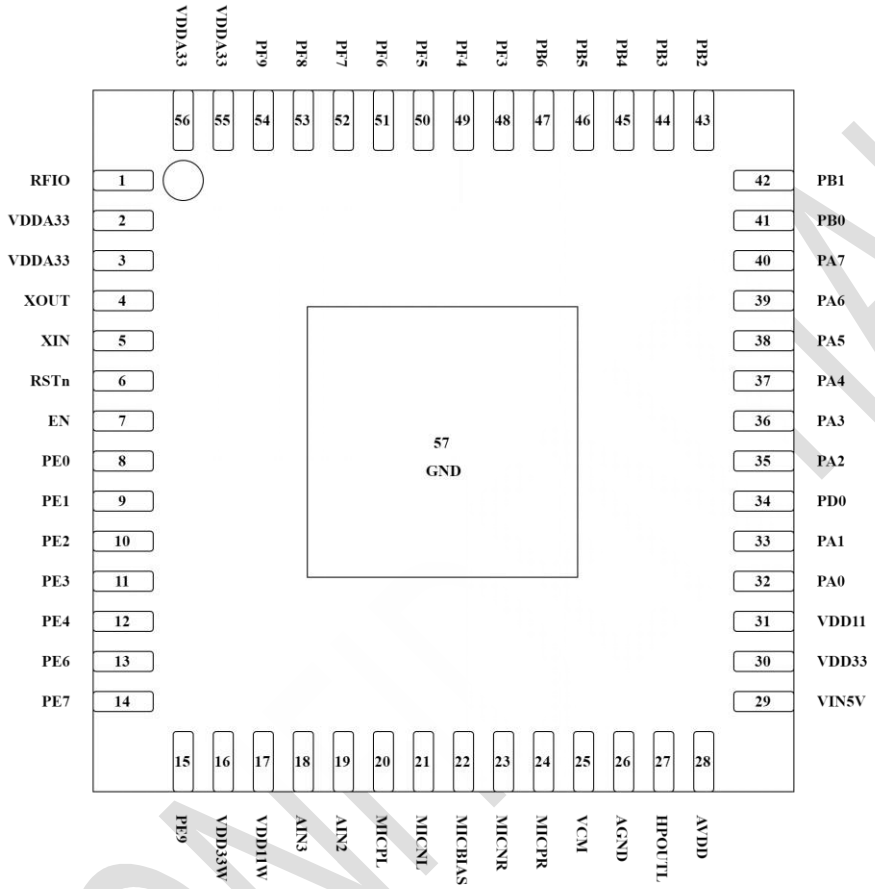
■ **PMU**

- Multiple high-performance LDOs are built in, and only one power supply device is needed for the periphery to work
- 5V Power supply, the power supply range supports a minimum of 3.6V input and a maximum of 5.5V input

- **Encryption and Decryption**
  - Built in AES-128/AES-192/AES-256 hardware encryption and decryption engine
  - Built in true random number generator
- **SAR ADC**
  - Support two input channel of 12bit SAR ADC with 1MHz sampling rate
- **Peripheral Interface and Timer**
  - Two UART interfaces with 3M baud rate maximum
  - One IIC interface, support IIC extended device
  - Six PWM interfaces, support direct driving for light control and motor applications
  - Four 32-bit timers inside
  - Built-in one independent watchdog(IWDG)
  - Built-in one window watchdog(WWDG)
- **GPIO**
  - Support 33 GPIOS
  - Except the GPIO of PD, other GPIOS can be configured with interrupt function
  - Some GPIOS with 5V tolerant capability
- **Development Support**
  - Provide software development package, application examples and notices
  - Content and services can be realized online, obtain address: https://platform.chipintelli.com
- **Firmware burning and protection**
  - Support firmware upgrade by UART and firmware protection
- **EMC and ESD**
  - Excellent EMC design and support FCC standard
  - Excellent ESD design, it can pass 4KV contact discharge test
- **ROHS and REACH**
  - Support ROHS and REACH standards
- **Packaging and Operating temperature**
  - Devices Packaging: QFN56, Length*Width*Thickness = 7*7*0.85 mm
  - Operating temperature: -40℃～+85℃

2 Pin Diagram and Function Description

2.1 Pin Diagram



2.2 Pin descriptions

Table 2-1 Pin descriptions

Pin number	Pin Name	Type	5V--Tolerant	Power on default state	Description Alternate functions
1	RFIO	IO	-	-	WIFI RF transmitter/receiver
2	VDDA33	P	-	-	WIFI 3.3V power supply, input capacitance is 4.7uF and 0.1uF
3	VDDA33	P	-	-	
4	XOUT	O	-	-	External 40MHz oscillator interface
5	XIN	I	-	-	External 40MHz oscillator interface
6	RSTn	I	-	-	Reset pin
7	EN	I	-	-	Enable WIFI function pin
8	PE0	IO	-	IN,PU	GPIO PE0 Note1
9	PE1	IO	-	IN,PU	GPIO PE1 Note1
10	PE2	IO	-	IN,PU	1. GPIO PE2 2. WIFI firmware download TX Note1
11	PE3	IO	-	IN,PU	1. GPIO PE3 2. WIFI firmware download RX Note1
12	PE4	IO	-	IN,PD	GPIO PE4 Note1
13	PE6	IO	-	IN,PD	GPIO PE6
14	PE7	IO	-	IN,PD	GPIO PE7
15	PE9	IO	-	IN,PU	1. GPIO PE9 2. WIFI BOOTMODE1 Note1/Note2
16	VDD33W	P	-	-	WIFI 3.3V power supply, input capacitance is 0.1uF
17	VDD11W	P	-	-	WIFI 1.1V power output, output capacitance capacitance is 0.1uF
18	AIN3	IO	-	IN,T+D	1. Reserved（Initial state at startup） 2. GPIO PC3 3. IIC SDA 4. PWM1 5. PDM DAT 6. SAR ADC input channel 3
19	AIN2	IO	-	IN,T+U	1. Reserved（Initial state at startup） 2. GPIO PC4 3. IIC_SCL 4. PWM0 5. PDM_CLK 6. SAR ADC input channel 2
20	MICPL	I	-	-	Left Microphone P input
21	MICNL	I	-	-	Left Microphone N input
22	MICBIAS	O	-	-	Microphone bias output
23	MICNR	I	-	-	Right Microphone N input
24	MICPR	I	-	-	Right Microphone P input
25	VCM	O	-	-	VCM Output
26	AGND	P	-	-	Analog ground
27	HPOUTL	O	-	-	DAC output
28	AVDD	P	-	-	3.3V output or 3.3V analog power supply, output capacitance/input capacitance is 4.7uF
29	VIN5V	P	-	-	VIN5V is the PMU power supply input pin. The normal working input voltage range is 3.6V-5.5V.

					A 4.7uf input capacitor is connected externally. The maximum input voltage of this pin is 6.5V. Note that over-voltage and surge protection devices need to be added, such as a TVS and a 4.7 ohm resistor to protect against surge impact
30	VDD33	P	-	-	3.3V output, output capacitance capacitance is 4.7uF
31	VDD11	P	-	-	1.1V output or 1.1V Power supply, output capacitance/input capacitance is 4.7uF
32	PA0	IO	-	-	GPIO PA0
33	PA1	IO	-	-	GPIO PA1
34	PD0	IO	√	IN,T+D	GPIO PD0
35	PA2	IO	√	IN,T+D	1. GPIO PA2(Initial state at startup) 2. IIS_SDI 3. IIC_SDA 4. PWM0
36	PA3	IO	√	IN,T+D	1. GPIO PA3(Initial state at startup) 2. IIS_LRCLK 3. IIC_SCL 4. PWM1
37	PA4	IO	√	IN,T+U	1. GPIO PA4(Initial state at startup)/PG_EN(Judge whether to upgrade firmware according to the level state of this pin at power on, the chip start the upgrading function at high power state of this pin) 2. IIS_SDO 3. PWM2
38	PA5	IO	√	IN,T+D	1. GPIO PA5(Initial state at startup) 2. IIS_SCLK 3. PDM_DAT 4. UART2_TX 5. PWM3
39	PA6	IO	√	IN,T+D	1. GPIO PA6(Initial state at startup) 2. IIS_MCLK 3. PDM_CLK 4. UART2_RX 5. PWM4
40	PA7	IO	√	IN,T+D	1. GPIO PA7(Initial state at startup) 2. PWM0 3. EXT_INT[0]
41	PB0	IO	√	IN,T+D	1. GPIO PB0(Initial state at startup) 2. PWM1 3. EXT_INT[1]
42	PB1	IO	√	IN,T+D	1. GPIO PB1(Initial state at startup) 2. PWM2 3. UART2_TX
43	PB2	IO	√	IN,T+D	1. GPIO PB2(Initial state at startup) 2. PWM3 3. UART2_RX
44	PB3	IO	√	IN,T+D	1. GPIO PB3(Initial state at startup) 2. PWM4 3. IIC_SDA
45	PB4	IO	√	IN,T+D	1. GPIO PB4(Initial state at startup) 2. PWM5 3. IIC_SCL
46	PB5	IO	√	IN,T+U	1. GPIO PB5(Initial state at startup) 2. UART0_TX 3. IIC_SDA 4. PWM1
47	PB6	IO	√	IN,T+U	1. GPIO PB6(Initial state at startup) 2. UART0_RX 3. IIC_SCL 4. PWM2
48	PF3	IO	-	IN,PD	GPIO PF3 Note1

49	PF4	IO	-	IN,PU	GPIO PF4	Note1
50	PF5	IO	-	IN,PU	GPIO PF5	Note1
51	PF6	IO	-	IN,PU	GPIO PF6	Note1
52	PF7	IO	-	IN,PU	GPIO PF7	Note1
53	PF8	IO	-	IN,PU	GPIO PF8	Note1
54	PF9	IO	-	IN,PU	GPIO PF9	Note1
55	VDDA33	P	-	-	WIFI 3.3V power supply, input capacitance is 4.7uF and 0.1uF	
56	VDDA33	P	-	-		
57	GND	P	-	-	GND	

Conformity with definition:

I Input

O Output

IO Bidirectional

P Power or ground

T+D Tristate plus pull-down

T+U Tristate plus pull-up

OUT Power-on defaults to output mode

IN Power-on defaults to input mode

Note1: PE/PF pin is only used as WIFI download firmware and debugging interface, and it is not recommended to be used for other purposes.

Note2: When the chip is powered on, the level of pin PE9(WIFI bootmode1) will be used as the WIFI upgrade mode judgment signal. When the power on level of this pin is high, the WIFI part will be directly started from the internal flash. When the power on level of this pin is low, the WIFI part will start the UART upgrade service. At this time, the supporting upgrade tool can be used to program the flash of the internal WIFI part of the chip.

Note3: The 57th pin of the chip is the heat dissipation pad on the bottom of the chip, which is also the grounding pad of the package and needs to be grounded.

2.3 Alternate functions

Table 2-2 Alternate functions

Pin Name	Function1	Function2	Function3	Function4	Function5	Analog Function	Specific Function
PA2	PA2	IIS_SDI	IIC_SDA	-	PWM0	-	-
PA3	PA3	IIS_LRCLK	IIC_SCL	-	PWM1	-	-
PA4	PA4	IIS_SDO	-	-	PWM2	-	PG_EN Note4
PA5	PA5	IIS_SCLK	PDM_DAT	UART2_TX	PWM3	-	-
PA6	PA6	IIS_MCLK	PDM_CLK	UART2_RX	PWM4	-	-
PA7	PA7	PWM0	-	EXT_INT[0]	-	-	-
PB0	PB0	PWM1	-	EXT_INT[1]	-	-	-
PB1	PB1	PWM2	UART2_TX	-	-	-	-
PB2	PB2	PWM3	UART2_RX	-	-	-	-
PB3	PB3	PWM4	IIC_SDA	-	-	-	-
PB4	PB4	PWM5	IIC_SCL	-	-	-	-
PB5	PB5	UART0_TX	IIC_SDA	PWM1	-	-	-
PB6	PB6	UART0_RX	IIC_SCL	PWM2	-	-	-
AIN3	-	PC3	IIC_SDA	PWM1	PDM_DAT	AIN3	-
AIN2	-	PC4	IIC_SCL	PWM0	PDM_CLK	AIN2	-

Note4: The PA4 pin is PG_En . It is pulled up by default. When the power on is judged to be high, the chip can automatically enter the upgrade mode when it detects an upgrade signal on UART0 when it is powered on. At this time, the supporting upgrade tool can be used to program the flash inside the chip. If no upgrade signal is detected on UART0, it will enter the normal working mode.

3 WIFI Characteristics

3.1 Supported frequency bands

Table 3-1 Frequency band table

Parameter	Min	Typ	Max	Unit
Receive frequency range 2.4GHz	2412		2484	MHz

3.2 Receiving characteristics

Table 3-2 Receiving characteristics table

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity					
11b,1M	FER<8%,1024 bytes		-94		dBm
11b,11M	FER<8%,1024 bytes		-87		dBm
11g,6M	FER<10%,1024 bytes		-90		dBm
11g,54M	FER<10%,1024 bytes		-74		dBm
11n,MCS0	FER<10%,1024 bytes		-90		dBm
11n,MCS7	FER<10%,1024 bytes		-71		dBm
Maximum input level					
11b	FER<8%,1024 bytes		4		dBm
11g	FER<10%,1024 bytes		-10		dBm
11n	FER<10%,1024 bytes		-10		dBm
Operating power consumption					
11b			80		mA
11g			82		mA
11n			82		mA

3.3 Emission characteristics

Table 3-3 Emission characteristics table

Parameter	Condition	Min	Typ	Max	Unit
Output power					
11b,1M DSSS	Maximum Burst power		18		dBm
11g,54M OFDM	Maximum Burst power		16		dBm
11n, MCS7	Maximum Burst power		14		dBm
Power consumption					
11b	100% Duty Cycle @17dBm		320		mA Note5
11g	100% Duty Cycle @14dBm		290		mA Note5
11n	100% Duty Cycle @13dBm		270		mA Note5

Note5: Test the current value of power supply VDDA33.

4 Electrical Characteristics

Table 4-1 Electrical Characteristics Table

Symbol	Description	Min.	Typical	Max.	Unit
VIN5V	PMU Power supply	3.6	5	5.5	V
AVDD	Analog Codec Power supply	2.97	3.3	3.63	V
VDD33	Chip IO Power Supply	2.97	3.3	3.63	V
VDD11	Chip core Power Supply Voltage	0.99	1.1	1.22	V
VDDA33	WIFI Power supply	2.97	3.3	3.6	V
VDD33W	WIFI IO Power supply	2.97	3.3	3.6	V
VIH	Input High Voltage, 3.0V ≤ VDD33 ≤ 3.6V	VDD33-0.6	/	VDD33+0.3	V
VIL	Input Low Voltage, 3.0V ≤ VDD33 ≤ 3.6V	/	/	0.6	V
VOL	Output Low Voltage @IOL = 12mA	/	/	0.4	V
VOH	Output High Voltage @IOH = 20mA	VDD33-0.5	VDD33	VDD33+0.3	V
$I_{3.3V}$	Chip 3.3V power supply working current	/	TBD	/	mA
$I_{1.1V}$	Chip 1.1V power supply working current	/	TBD	/	mA
TA	Chip Operating temperature	-40	/	+85	℃
T_{ST}	Chip Storage temperature	-55	/	+150	℃

5 Packaging Information

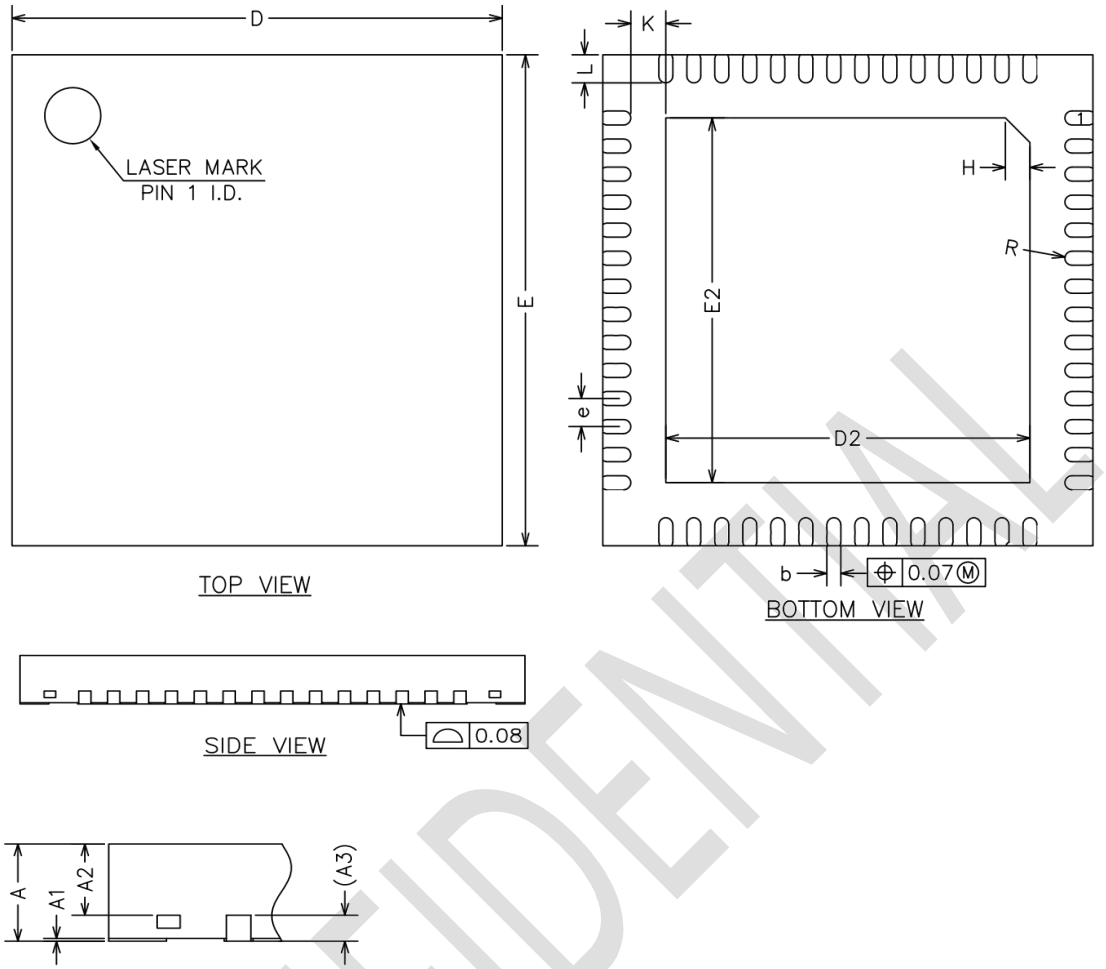


Table 5-1 Packaging Table

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
A2	0.60	0.65	0.70
A3		0.20REF	
b	0.15	0.20	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	5.10	5.20	5.30
E2	5.10	5.20	5.30
e	0.30	0.40	0.50
H		0.35REF	
K		0.50REF	
L	0.35	0.40	0.45
R	0.09	-	-

6 Order Information

Table 6-1 Order Information Table

Orderable Device	Flash	Status	Package Type	Pins	Package Qty	Eco Plan	MSL Peak Temp	Op Temp (°C)
CI2305	4MByte	MP	QFN56/Tape	56	2600	RoHS & Green	Level-3 260C-UNLIM	-40 to 85
CI2306	6MByte	MP	QFN56/Tape	56	2600	RoHS & Green	Level-3 260C-UNLIM	-40 to 85

Due to the small Flash capacity, CI2305 only supports offline speech recognition and IOT connected for AIOT applications. CI2306 can support offline+online speech recognition, and supports larger capacity neural network models and more sound playback, with better noise reduction effect.

7 Application

7.1 Application Reference Circuit Diagram

The periphery of CI1306 chip only needs a few devices to support all kinds of voice applications. The chip can support dual microphone input or single microphone input can AEC echo cancellation function. Users can select the appropriate circuit according to the function, power consumption and cost requirements of the designed application scheme. The application of a single microphone input & AEC echo cancellation scheme of the chip is described in detail below.

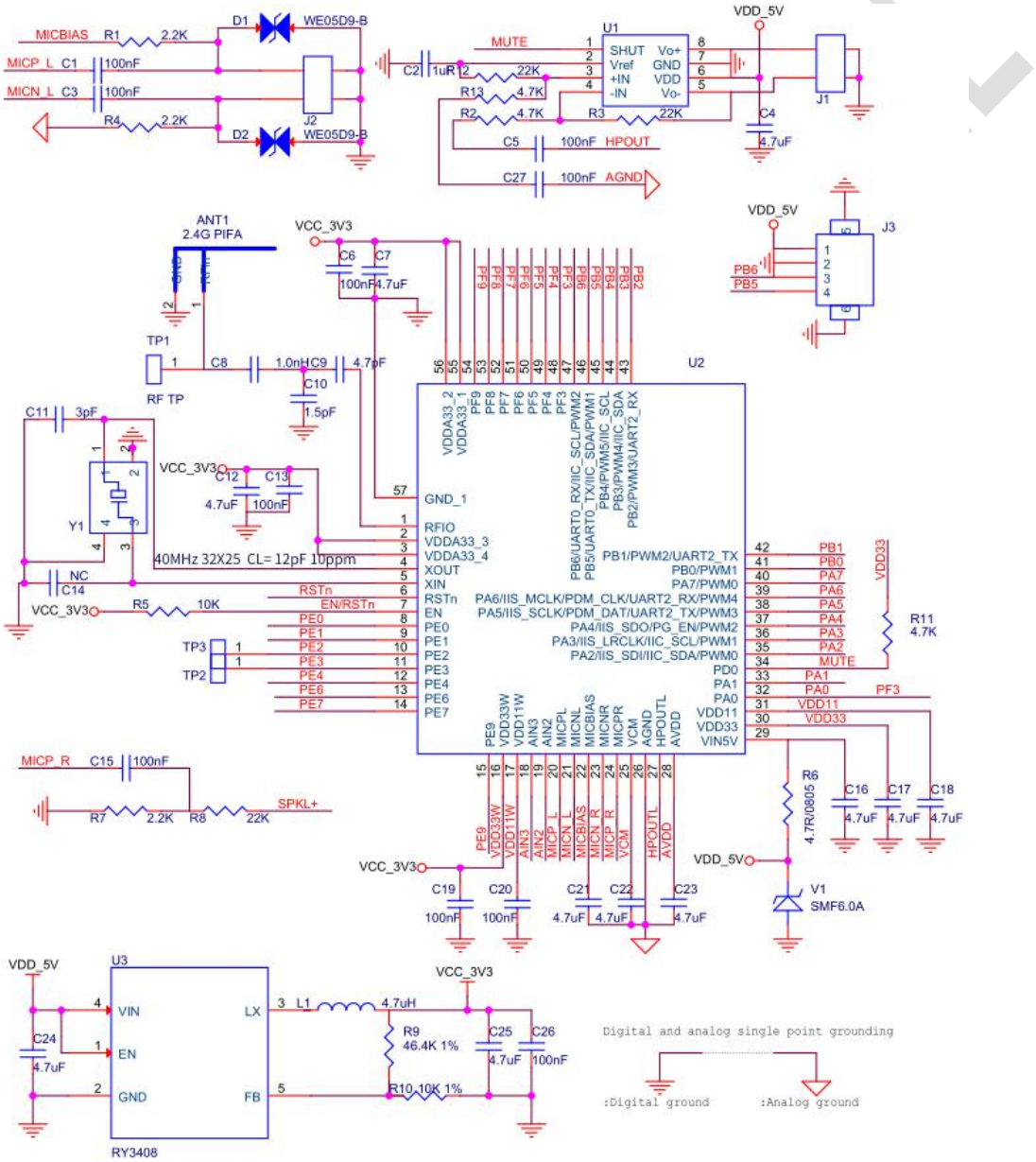


Diagram 7-1 CI230X's application reference circuit diagram

The above figure is the circuit diagram of an application scheme of CI230X supporting single microphone input & AEC echo cancellation and power amplifier output. The chip can use 5V direct power supply, and users can design according to the corresponding peripheral device specifications in the figure above. External crystal oscillator is recommended for the chip, but the chip also has built-in RC oscillator. When there are high requirements to reduce cost and few algorithm support functions, the internal RC oscillator can be directly used.

If the online upgrade function is to be considered in the schematic design, the UART0 pin can be led out, to facilitate the firmware upgrade of the flash inside the main chip through UART0. The PA4 (PG_EN) pin of the chip is internally pulled up, and the power on defaults state is the upgrade mode. After power on, the chip detect the upgrade signal from the external UART0 port, and directly start the upgrade. The default startup time of the chip is about 850ms with extending due to the detection of upgrade mode. If the user has high requirements for the startup time, the PA4 pin can be led out, two 2.2kΩ pull-down resistors can be added to the ground, and a test point is added in the middle of the two 2.2kΩ resistors. At this time, the chip's startup state is in the normal mode, and the startup time is about 350ms, which can shorten the startup time. If you want to upgrade online at this time, you can supply high level to the intermediate test points connected by two 2.2kΩ resistors externally, pull PA4 pin up, and then upgrade through UART0.

The chip scheme can choose differential microphone design or single ended microphone design. The differential microphone design in the figure above is recommended. If the user has requirements to reduce the cost, the microphone part in the figure above can be modified to the single ended microphone design, which can use less passive devices than the differential microphone. However, this method is only recommended to be used when the microphone line length is less than 20cm. Otherwise, because the line is too long and the anti-interference effect is not enough, the speech recognition effect is not as good as that of the differential microphone design. The power amplifier in the figure above adopts class AB power amplifier, and 8002 power amplifier chip is recommended. Users can also choose the power amplifier chip according to the requirements of the scheme. If the power amplifier function is not required, this part of the circuit can also be removed to reduce the cost. If users do not use AEC echo cancellation function, they can also remove this part of the circuit to reduce the cost.

If the user has no special requirements to reduce the power consumption, it is recommended to directly use the PMU inside the chip for power supply. If there are requirements to reduce the power consumption, an external DCDC chip can be added to supply power to the chip at 1.1V to reduce power consumption. The UART ports of the chip support 5V communication. The UART0 port in the figure above is connected with a 3.3V signal. If 5V is to be connected, add a pull-up resistance connected to 5V around the RX and TX pins of UART0 without adding an additional

voltage conversion circuit.

The VDDA33 and VDD33W pins of this chip are WIFI power supply input pins. In the figure above, DCDC power supply is used with recommended DCDC chip by RY3408. Users can also choose DCDC chip by themselves according to the requirements of the scheme. The current drive capability of DCDC chip must be greater than 1A, and only power to WIFI part to ensure stable performance.

Both RSTN and EN pins of the chip can be used to reset WIFI functions. It is recommended to use the EN pin in the above figure when resetting. The pins PE2 and PE3 of the chip are WIFI firmware upgrade UART port by default, and the pin PE9 is WIFI firmware download enable port by default. When upgrading WIFI firmware, user need to connect PE2 and PE3 pins to the UART port, pull PE9 pin down to the ground, and then power on the chip to make the chip enter the upgrade mode, and then you can upgrade firmware through the upgrade software provided by Chipintelli.

The oscillator specification used in the periphery of the chip is 40MHz cl=12pf 10ppm, which requires an external 3pF capacitor on the XOUT pin. The parameters and specifications of this oscillator cannot be changed at will. Please strictly follow the design in the schematic diagram.

The RFIO pin of the chip is an antenna pin, and a level-1 T-type matching network circuit is reserved in the above figure. Users can reserve matching network circuit for chip and antenna end according to the actual stacking condition of PCB and antenna specification. Different PCB stacks, antenna specifications and different environments of PCBA assembly require separate debugging of the matching network circuit to ensure RF performance.

7.2 Other Application Notices

1. The chip integrates a PMU management unit, which contains multiple LDOs to provide 3.3V and 1.1V voltages to the chip respectively. The ripple of external 5V power supply shall be less than 300mV. If the requirements for RF performance and power consumption are high, it is recommended that the external power chip supply VDDA33 and VDD33W separately.

2. RF devices are sensitive to oscillator frequency offset. If the working environment of the product is poor, it is recommended to choose wide temperature oscillator; At the same time, if the PCB is a multi-layer board, it is recommended to excavate under the oscillator of adjacent layers to reduce the influence of parasitic capacitance on oscillator frequency offset.

3. The RFIO pin must reserve a matching network circuit, and the wiring must be impedance

matched. If the cable is too long, it is recommended to reserve a matching network circuit near the antenna.

4. If the product needs to playback audio, AGND and HPOUTL pin should be connected to the power amplifier in the way of differential wiring to avoid audio interference and abnormal noise.

5. The chip is lead-free. When SMT soldering, please set parameters such as furnace temperature and time according to lead-free standard.

6. We should pay attention to the electrostatic effect when we use and pack chips. It is suggested that antistatic materials be used for isolation.