CI23162 Data sheet

Cost-effective neural network intelligent voice chip

- **Brain Neural Network Processor (BNPU)**

-BNPUV3.5, which supports DNN\TDNN\RNN\CNN and other neural networks and parallel vector operations, can realize high-performance speech recognition and call noise reduction functions

- **CPU and memory**

-CPU frequency up to 210 MHz
-Built-in 2MBytes Flash memory
-Built-in 288KBytes SRAM
-Built-in 256bit eFuse for application encryption

- **Audio Codec**

-High performance and low power consumption audio ADC, SNR ≥ 95dB

-Low power consumption audio DAC, SNR ≥ 95dB

- **PWM**

-Supports 3 PWM interfaces

- **GPIO**

-3 high-speed GPIO with a switching frequency of up to 20MHz
-2 GPIO channels support 5V level communication

- **Reset and power management**

-Power supply voltage range 3.6V~5.5V
-Built-in PMU power management unit
-Built-in power-on reset (POR)
-Built-in voltage detection (PVD)

- **clock**

-Built-in RC oscillator
--Bluetooth external crystal oscillator input

- **communication interface**

-1 IIC interface
-1 UART interface, supports 5V level communication, up to 3Mbps communication rate

- **Timer and watchdog**

-Built-in 2 sets of 32-bit timers and 1 watchdog

- Wireless features

-Bluetooth 5.4

- +5 dBm Maximum TX power

-98 dBm RX sensitivity @ BLE 1 Mbps

Catalogue

1 Description

1.1 Functional description

The CI23162 is a next-generation high-performance neural network smart voice Bluetooth chip developed by Qiyintelun. It integrates the company's proprietary Brain Neural Network Processor (BNPU) V3.5 and CPU core, delivering a system clock rate of up to 210MHz. Featuring 288KB of built-in SRAM, it incorporates a Power Management Unit (PMU) and RC oscillator, along with a single-channel high-performance low-power Audio Codec and multiple peripheral control interfaces including UART, I2C, PWM, and GPIO. The chip also supports Bluetooth Low Energy (BLE) connectivity. With minimal external components like resistors and capacitors, the CI23162 enables flexible hardware solutions for smart voice products, offering exceptional cost-effectiveness.

CI23162 adopts industrial grade design standard, has good environmental reliability, its working temperature range is-40℃~+85℃, in line with MSL3 grade humidity sensitivity, in line with IEC 61000-4-24KV contact discharge test standard, in line with RoHS and REACH environmental protection standards.

The CI23162 leverages Qintai Lun's next-generation BNPU technology, which supports neural networks including DNN, TDNN, RNN, and CNN, along with parallel vector operations. This enables high-performance speech recognition, noise reduction, and exceptional environmental noise suppression capabilities. The device also features Bluetooth BLE5.4 support for remote control via mobile app mini-programs. With support for multiple global languages including Chinese, English, and Japanese, the CI23162 solution finds wide application in home appliances, lighting systems, toys, wearables, industrial equipment, and automotive sectors, facilitating voice interaction and control for various intelligent voice applications.

1.2 Chip specifications

The function block diagram of CI23162 is shown in Figure 1-1:

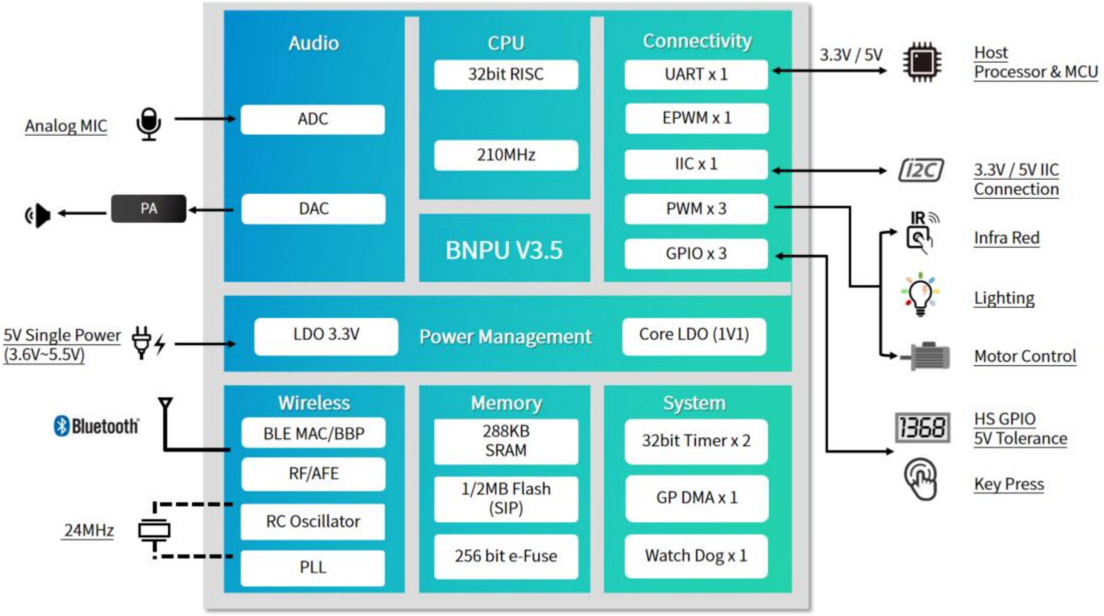


Figure 1-1 CI23162 function block diagram

- **Brain neural network processor BNPU V3.5**

-BNPU V3.5 support DNN \ TDNN \ RNN \ CNN and other neural networks and parallel vector operations. It can realize high-performance speech recognition, speech noise reduction and other functions

- **CPU**

-32-bit high-performance CPU, up to 210MHz operating frequency

- **Memory**

-Built-in 288KB SRAM

-Built-in 256bit eFuse

-Built-in 2MB Flash

- **PDA**

-Support Bluetooth 5.4

- +5 dBm Maximum TX power

- -98 dBm RX sensitivity @ BLE 1 Mbps

- -100 dBm RX sensitivity S2

- -103 dBm RX sensitivity S8

- **Audio interface**

-Built-in high performance low power Audio Codec module, supporting single channel ADC sampling and single channel DAC playback

-Support for Automatic Level Control (ALC) function

-Support for 8kHz/16kHz/24kHz/32kHz/44.1kHz/48kHz sampling rate

- **Power management unit PMU**

-Support wide power supply voltage, power supply range 3.6V~5.5V

-Built-in 2 high-performance LDO circuits, no need to configure external power chip. The module board only needs a small number of peripheral components

- **Clock**

-Built-in RC oscillator

-Bluetooth external crystal oscillator input

- **Peripheral and timer**

-1 UART interface, supporting communication at the highest baud rate of 3M

-1 IIC interface, which can be connected to external IIC devices for expansion

-3 PWM interfaces, which can be directly driven for lamp control and motor applications

-2 built-in 32bit timers

-Built-in 1 independent watchdog (IWDG)

- **GPIO**

-Supports 3 GPIO ports and can be used as main control IC

-Each GPIO port can be configured with interrupt function and pull-up/down state

-2 GPIO channels can directly support 5V level communication through external 5V pull-up resistor

- **Software development support**

-Provide complete software development kit, application solution examples. For firmware quick development online and other support, please visit: https://aiplatform.chipintelli.com for details

- **Firmware flashing and protection**

-Support UART upgrade and firmware protection

- **ESD function**

-Adopted internal ESD enhanced design, can pass the 4KV contact discharge test

- **ROHS and REACH**

  -Use of environmentally friendly materials, support RoHS and REACH standards

- **Packaging and operating temperature range**

  -Packaging: SOP16, size: 9.9mmX6.0mmX1.7mm

  -Working environment temperature: -40℃~+85℃

2 Pin diagram and function description

2.1 Pin diagram

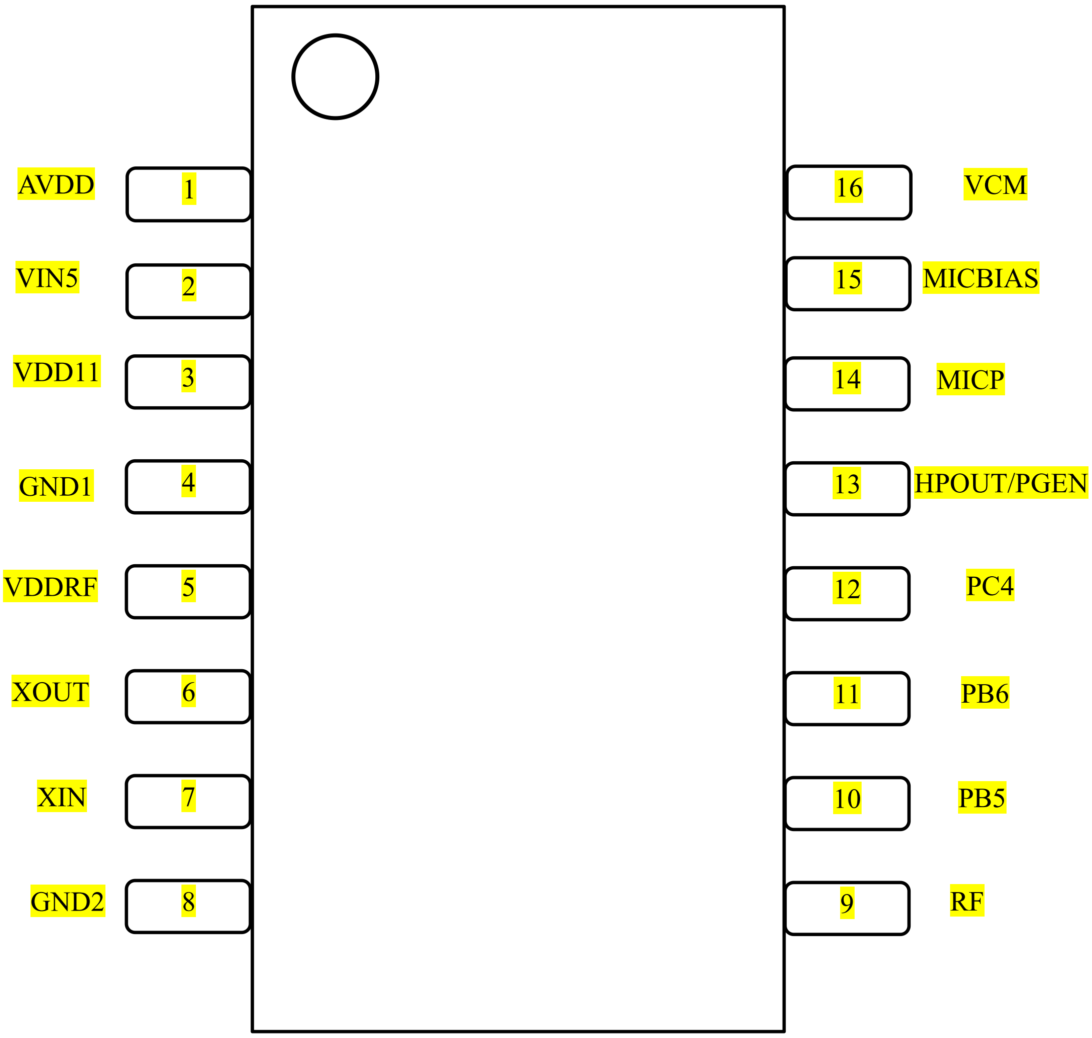


Figure 2-1 CI23162 pin order and definition

2.2 Pin description

Pin description is shown in Table 2-1

Pin number	Pin Name	Type	5V--Tolerant	Power on default state	Description Alternate functions
1	AVDD	P	-	-	● Internal LDO-3.3V Output ● Internal analog circuitry is powered by 3.3V input * Note1*
2	VIN5V	P	-	-	● Power supply voltage input, power supply voltage range 3.6V~5.5V * Note1*
3	VDD11	P	-	-	● LDO-1.1V output ● The kernel is powered by 1.1V input * Note1*
4	GND1	P	-	-	● Ground
5	VDDRF	P	-	-	● RF power input
6	XOUT	IO	-	-	● Jewelstone output
7	XIN	IO	-	-	● Jewelstone input
8	GND2	P	-		● Ground
9	RF	IO	-		● RF antenna
10	PB5	IO	√	IN，T+U	● GPIO PB5 (default state on power-on) ● UART0_TX ● IIC_SDA ● PWM1 ● PWMP
11	PB6	IO	√	IN，T+U	● GPIO PB6 (default state on power-on) ● UART0_RX ● IIC_SCL ● PWM2 ● PWMN
12	PC4	IO	-	IN，T+U	● Retained (default state on power-on) ● PC4 ● SCL ● PWM0
13	HPOUT/PGEN	O	-	-	● DAC output ● *PGEN Note2*
14	MICP	I	-	-	● Microphone P input
15	MICBIAS	O	-	-	● Microphone bias output
16	VCM	O	-	-	● VCM POWER Output

Note1 The pin needs to be connected to a 4.7uF capacitor

Note2 When the power is on, this pin is detected as high level, and the system will enter programming mode. By default, this pin is low level

Symbol definition

I	input
O	output
IO	bidirectional
P	power or ground
T+D	Tri-state pull-down
T+U	Tri-state pull-up
OUT	power-on defaults to output mode
IN	power-on defaults to input mode

All IOs can be configured with drive capability and pull-up/down status.

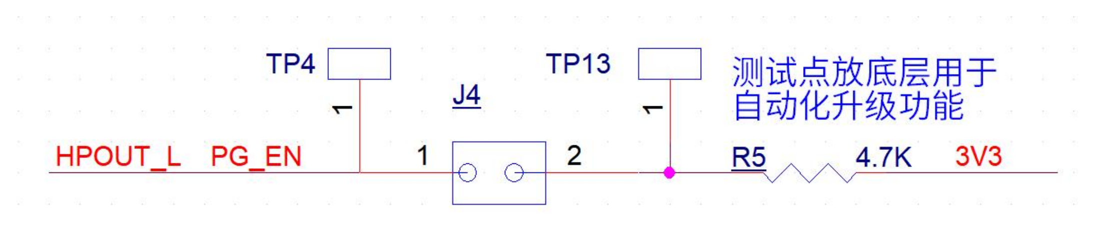
2.3 Function multiplexing

Table 2-2 IO multiplexing function

Pin Name	Function1	Function2	Function3	Function4	Function5	Function6	Specific Function
PB5	PB5	UART0_TX	IIC_SDA	PWM1	PWMP		
PB6	PB6	UART0_RX	IIC_SCL	PWM2	PWMN		
PC4	-	PC4	SCL	PWM0			

The HPOUT/PGEN pin on C23162 is pre-configured with a pull-down resistor within the chip. During power-on, the system detects whether this pin is pulled up to 3.3V high level by an external pull-up resistor. If the high level is detected and an upgrade signal from UART0 is present, the system enters upgrade mode. If no external pull-up resistor is connected to this pin, the system skips the upgrade mode detection phase during power-on and directly enters normal startup mode for rapid boot. For applications requiring fast boot, the HPOUT/PGEN pin can be routed out with a jumper wire, then connected to a 4.7K Ω resistor to pull up to 3.3V power supply. This configuration enables normal functionality during power-on, reducing boot time to approximately 350ms. To enable online upgrades, short-circuit the jumper wire or its test points to pull the PGEN pin to 3.3V high level via UART0 port. For non-fast-boot applications, the PGEN pin can be directly pulled up using the 4.7K Ω resistor. Detailed implementation methods should follow the reference application diagram or consult our FAE. The two operating modes of PGEN are listed in the table below:

J4 state	Description
Open circuit	The system enters normal operation mode upon power-up, with a startup time of approximately 350 ms. By shorting the test points before power-up, the system can enter upgrade mode instead. This is suitable for products with strict power-up time requirements.
Short circuit	Upon power-up, the system defaults to upgrade mode, with a startup time of approximately 850 ms. After the upgrade is completed, disconnecting J4 switches the system to functional mode, which has a startup time of approximately 350 ms.



3 Electrical character

Table 3-1 Electrical characteristics table

Symbol	Description	Min.	Typical	Max.	Unit
VIN5V	Chip power input *Note1*	3.6	5.0	5.5	V
AVDD	3.3V power supply	2.97	3.3	3.63	V
VDD11	1.1V power supply	0.99	1.1	1.21	V
V_{IH}	Enter a high level （3.0V ⩽VDD33 ⩽ 3.6V）	0.7 × VDD33	-	VDD33+0.3	V
V_{IL}	Enter a low level （3.0V ⩽ VDD33 ⩽ 3.6V）	-0.3	-	0.3 × VDD33	V
V_{OL}	Output low level @IOL = 12mA	-	-	0.4	V
V_{OH}	Output high level @IOH = 20mA	2.4	-	-	V
I_{5V-IO}	Drive current at 3.3V when the 5V voltage is output from the IO port	20	-	33	mA
I_{3V3-IO}	3.3V withstand voltage IO port output 3.3V drive current	14	-	24	mA
Σ IVDD	The total current of all IOs on the chip	-	-	99	mA
Pde	The chip uses 5V power supply and VDD11 is supplied with 1.1V externally. The total power consumption of 5V power supply (TA =25° C) is normal when the identification is performed	80	-	140	mW
Pdi	The chip uses 5V power supply and the system uses internal LDO power supply. The total power consumption of 5V input is normal identification (TA = 25 ° C)	160	-	310	mW
RC precision *Note2*	TA：-40℃～+85℃	-1.5	-	+1.5	%
f_{XTAL}	Bluetooth crystal oscillator input		24		Mhz
Top	Chip operating temperature	-40	-	+85	℃
Tst	Chip storage temperature	-55	-	+150	℃

Note 1: The ripple is required to be less than 300mVp-p.

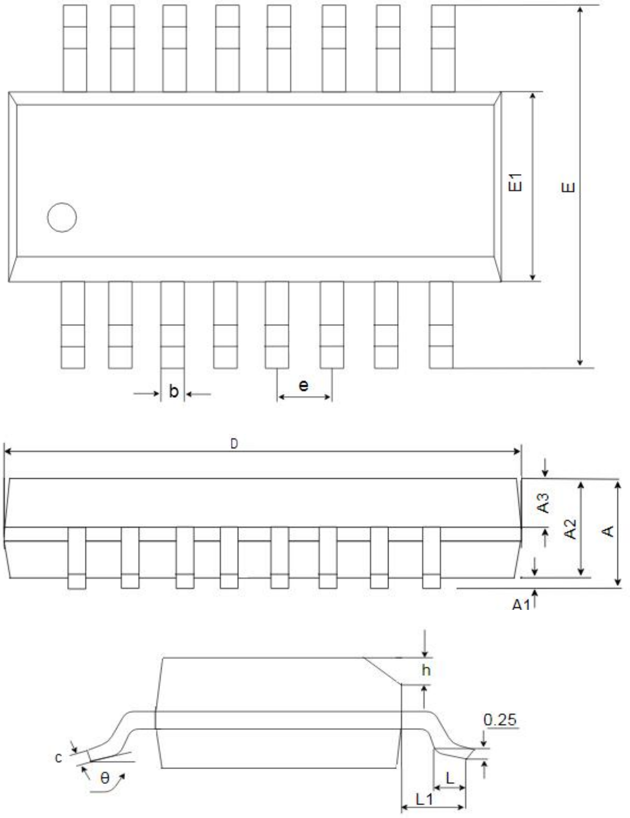
Note 2: Due to the inherent principles and characteristics of semiconductor technology, the built-in RC oscillator in chips may exhibit temperature drift (±1.5%) in high/low temperature environments. The CI23162 chip incorporates a baud rate adaptive circuit that ensures stable communication between the chip and host computer under extreme temperatures. For applications requiring ultra-precise clock synchronization, please utilize our externally oscillated chip configuration with corresponding implementation solutions.

Table 3-2 Bluetooth characteristics table

No	Parameter	Symbol	Conditions	MIN	TYP	MAX	UNIT
1	Sleep Power	I_SLEEP	VDDRF=3.3V		6		uA
2	Current in TX 0dBm	I_TX	VDDRF=3.3V		2.5		mA
3	Current in RX 1Mbps BLE	I_RX	VDDRF=3.3V @ -98 dBm sensitivity		2.8		mA
4	Frequency range	Freq		2300		2600	Mhz
5	Output power	Pout		-20		5	dBm

The above power consumption data was measured when VDDRF is equal to 3.3V

4 Packaging information



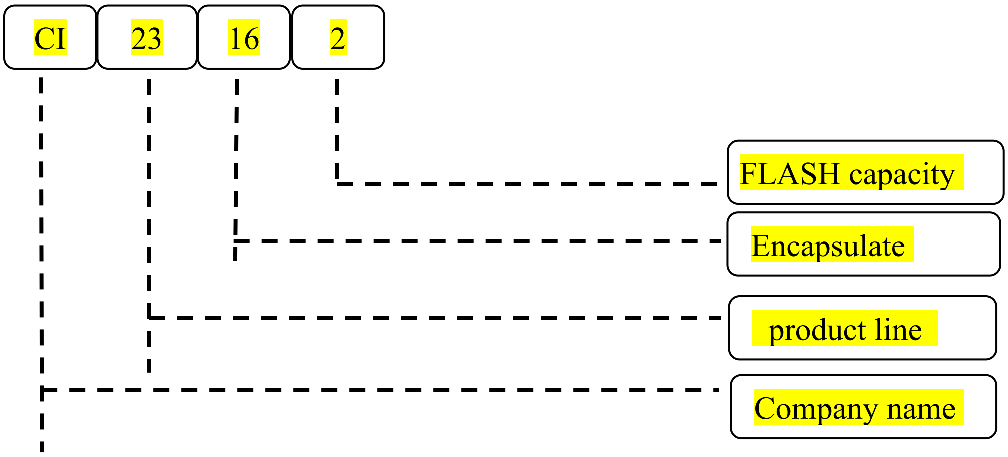
COMMON DIMENSIONS

SYMBOL	UNIT：MILLIMETER		
	MIN	NOM	MAX
A	_	_	1.70
A1	0.10	_	0.225
A2	1.30	1.40	1.50
A3	0.6	0.65	0.70
b	0.39	_	0.47
c	0.20	_	0.24
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	_	0.50
L	0.50	0.6	0.80
L1	1.05REF		
θ	0	_	8°

5 Order information

The Mark of CI23162 chip package is shown in the figure below. The first line is the company LOGO, the second line is the chip model, the third line is the production batch number, and the dot in the lower left corner is the identification of pin 1.

The chip model is defined as follows:



The order information of CI23162 chip is shown in Table 5-1.

Chip Model	Package Type	Basic packaging	Package Qty	Ex-factory packaging	Standard Pack Qty
CI23162	SOP16	Pipe installation	50pcs	box-packed	10000pcs （200 tubes/box）

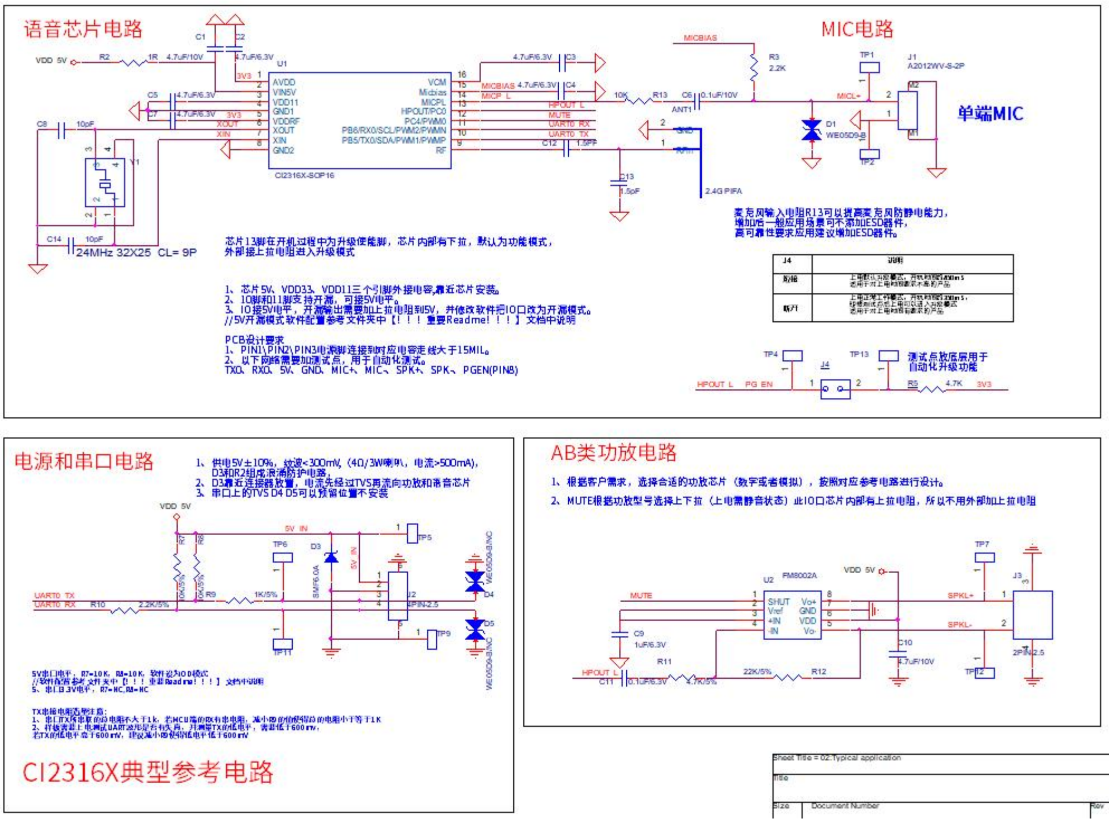
Table 5-1 CI23162 chip order information table

6 Application

6.1 Application reference circuit diagram

The CI23162 chip requires only a small number of peripheral components to develop product solutions that support various voice applications. The CI23162 supports single microphone and single-ended input. Application design can select appropriate circuit designs based on functional requirements, power consumption, cost, and other factors.

The following is a typical application solution of CI23162, which introduces the key points and precautions of application solution design.



麦克风输入电阻R13可以提高麦克风防静电能力，
增加后一般应用场景可不添加ESD器件，
高可靠性要求应用建议增加ESD器件。

芯片13脚在开机过程中为升级使能脚，芯片内部有下拉，默认为功能模式，
外部接上拉电阻进入升级模式

1、芯片5V、VDD33、VDD11三个引脚外接电容,靠近芯片安装。
2、10脚和11脚支持开漏，可接5V电平。
3、IO接5V电平，开漏输出需要加上拉电阻到5V，并修改软件把IO口改为开漏模式。
//5V开漏模式软件配置参考文件夹中【！！！重要Readme！！！】文档中说明

PCB设计要求
1、PIN1\PIN2\PIN3电源脚连接到对应电容走线大于15MIL。
2、以下网络需要加测试点，用于自动化测试。
TX0、RX0、5V、GND、MIC+、MIC-、SPK+、SPK-、PGEN(PIN8)

测试点放底层用于
自动化升级功能

1、供电5V±10%，纹波<300mV,（4Ω/3W喇叭，电流>500mA),
D3和R2组成浪涌防护电路，
2、D3靠近连接器放置，电流先经过TVS再流向功放和语音芯片
3、串口上的TVS D4 D5可以预留位置不安装

5V串口电平，R7=10K，R8=10K，软件设为OD模式
//软件配置参考文件夹中【！！！重要Readme！！！】文档中说明
5、串口3.3V电平，R7=NC,R8=NC

1、根据客户需求，选择合适的功放芯片（数字或者模拟），按照对应参考电路进行设计。
2、MUTE根据功放型号选择上下拉（上电需静音状态）此IO口芯片内部有上拉电阻，所以不用外部加上拉电阻

Figure 6-1 Reference circuit diagram of typical application solution of CI2316X

The diagram above illustrates a reference design circuit for the CI2316X series chips (including CI23162), demonstrating a typical application scenario featuring a single microphone with single-ended input and power amplifier output. This design is not limited to specific terminal products. When developing application solutions, engineers should prioritize compatibility with host computer terminals by downloading reference schematics and PCB layouts from Chipinelli Documentation Center and AI Platform based on the terminal's functional requirements and performance specifications. Documentation Center link: https://document.chipintelli.com/

If the board-level upgrade function needs to be reserved during application solution design, UART0 pins can be led out as sockets or test points, so that the firmware can be flashed or upgraded through UART0 after PCB board patching.

The power amplifier configuration of this typical application solution is AB class power amplifier, and the 8002 series power amplifier is recommended. If the voice prompt function is not required, the circuit part can be removed to reduce the cost of the solution.

If the application solution does not require ultra-low power consumption, it is recommended to use the internal PMU of CI23162 to reduce the cost. If the application solution requires ultra-low power consumption, the external DCDC circuit can be used to supply 1.1V power to CI23162 to reduce the system power consumption.

The UART port of CI23162 can support 5V level communication. If the application solution needs to connect to 5V communication level, it is recommended to use the serial port design in the figure above. It is only necessary to add a 5V pull-up resistor around the RX and TX pins of UART0, without configuring the level conversion circuit.

The crystal oscillator specification of CI23162 is 24MHZ, CL is 9pF, and the matching capacitor is 10pF. The parameters of this crystal cannot be changed at will.

The antenna design of CI23162 should refer to the standard solution of Chipinelli. The matching capacitor should be selected with recommended parameters and placed as close as possible to the RF foot. The PCB antenna area should be cleared and the integrity of the reference plane should be guaranteed, and it should be far away from metal devices to avoid affecting the antenna performance.

6.2 Other application notes

1. CI23162 is manufactured with lead-free and environmentally friendly materials. When SMT welding, please set the reflow temperature and time parameters according to lead-free standards as shown in the figure below

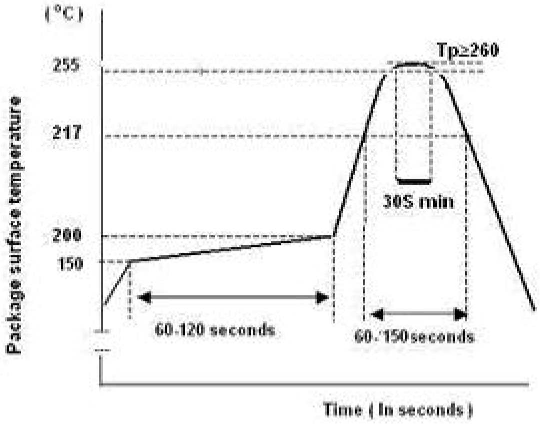


Figure 6-2 Furnace temperature curve

2. Attention should be paid to the use, handling and production of CI23162 with anti-static measures, and its packaging should be made of anti-static materials.

- Chipinelli reserves the right to interpret and modify this specification. If modified, no further notice will be given! Customers should obtain the latest version of the information before application design and verify whether the relevant information is accurate and complete.
- Any semiconductor product may fail or malfunction under certain conditions. The chip application party is responsible for complying with safety standards and taking safety protection measures when using the product for system design and complete machine manufacturing, so as to avoid personal injury or property loss caused by possible product failure!
- Chipinelli will be committed to providing customers with better products and better services!